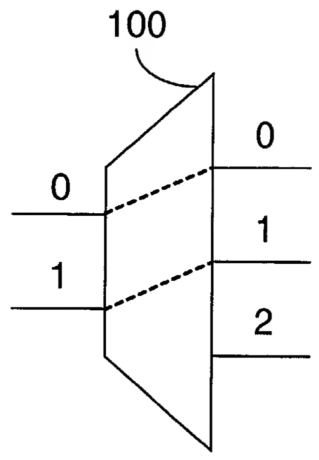


FIG. 1A

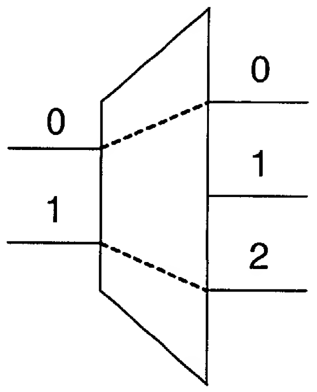


FIG. 1B

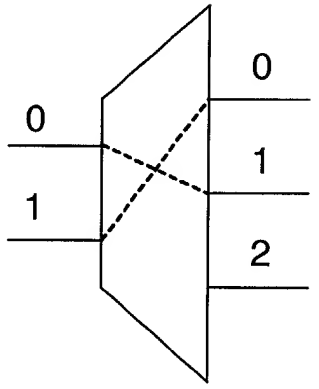


FIG. 1C

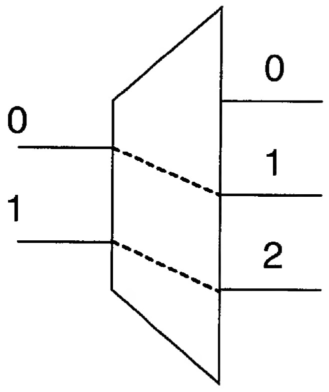


FIG. 1D

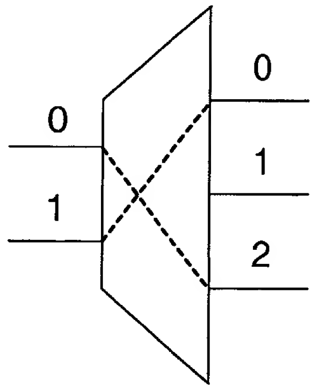


FIG. 1E

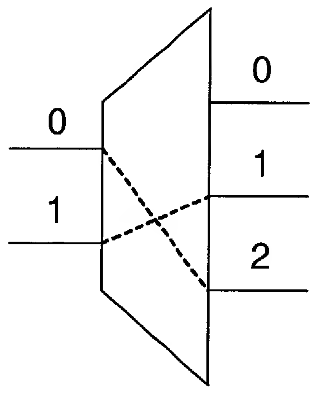


FIG. 1F

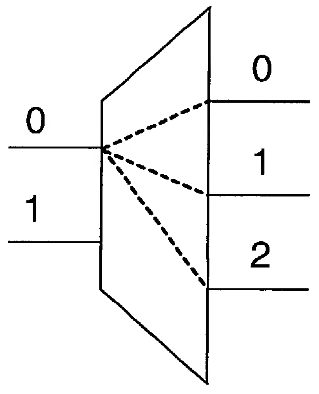


FIG. 1G

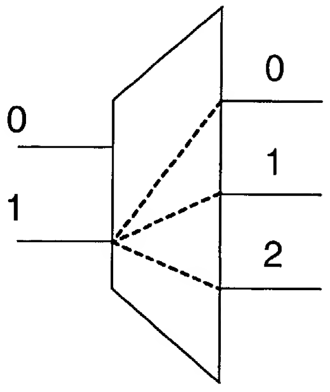


FIG. 1H

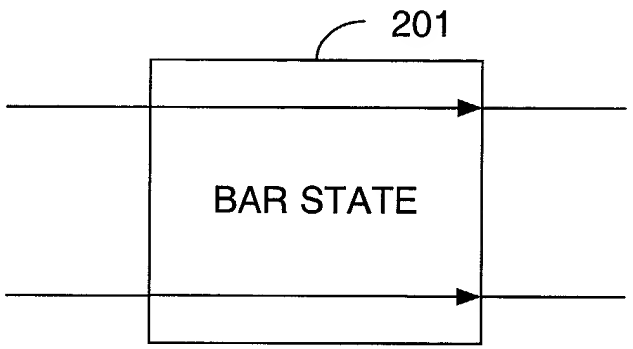


FIG. 2A

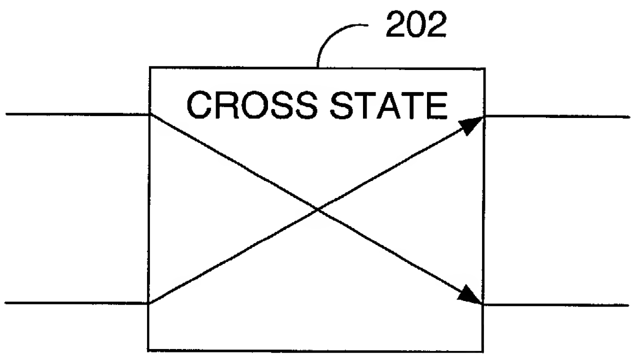


FIG. 2B

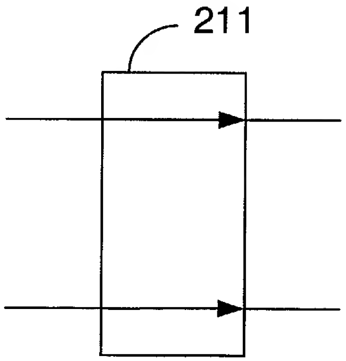


FIG. 2C

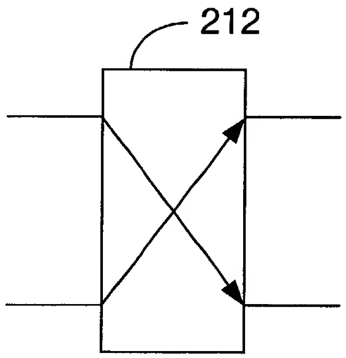


FIG. 2D

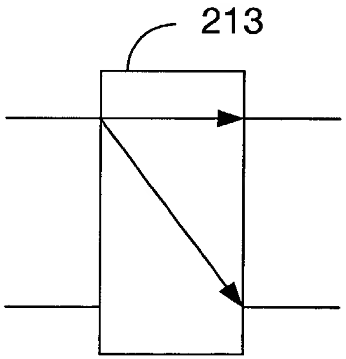


FIG. 2E

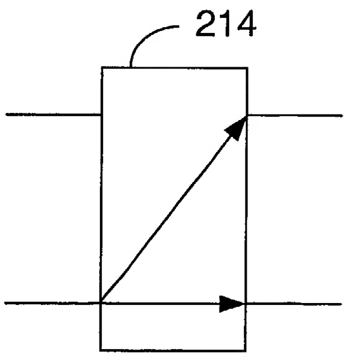


FIG. 2F

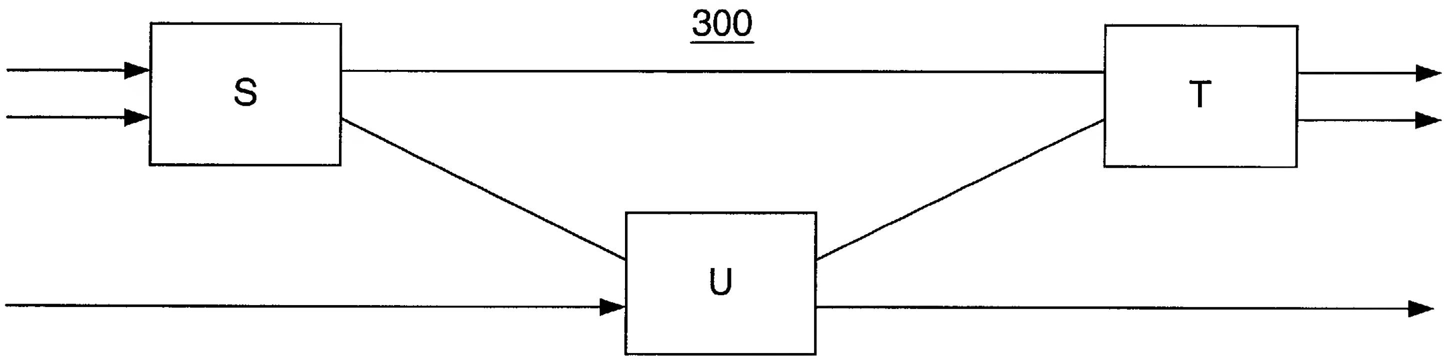


FIG. 3A

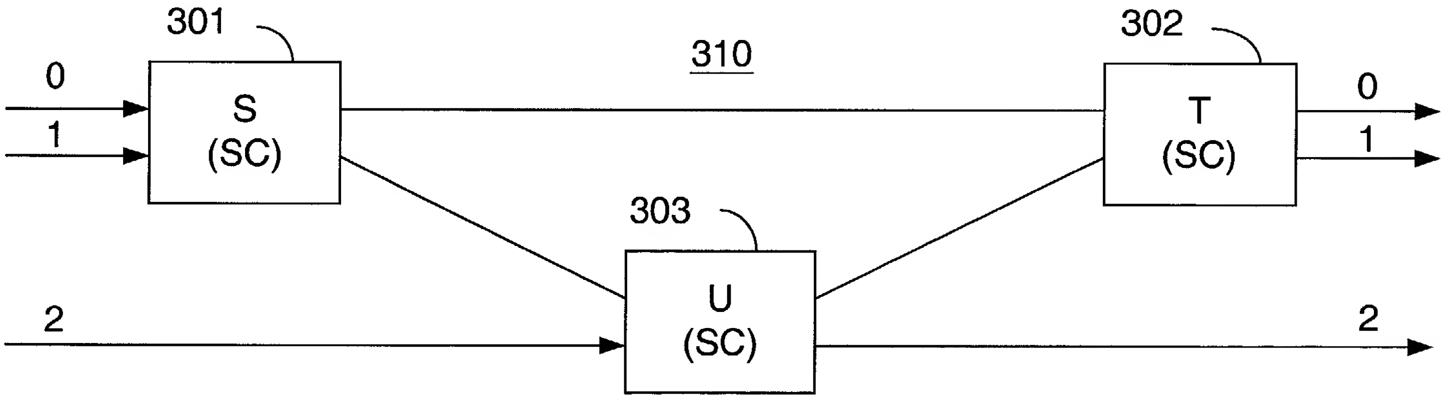


FIG. 3B

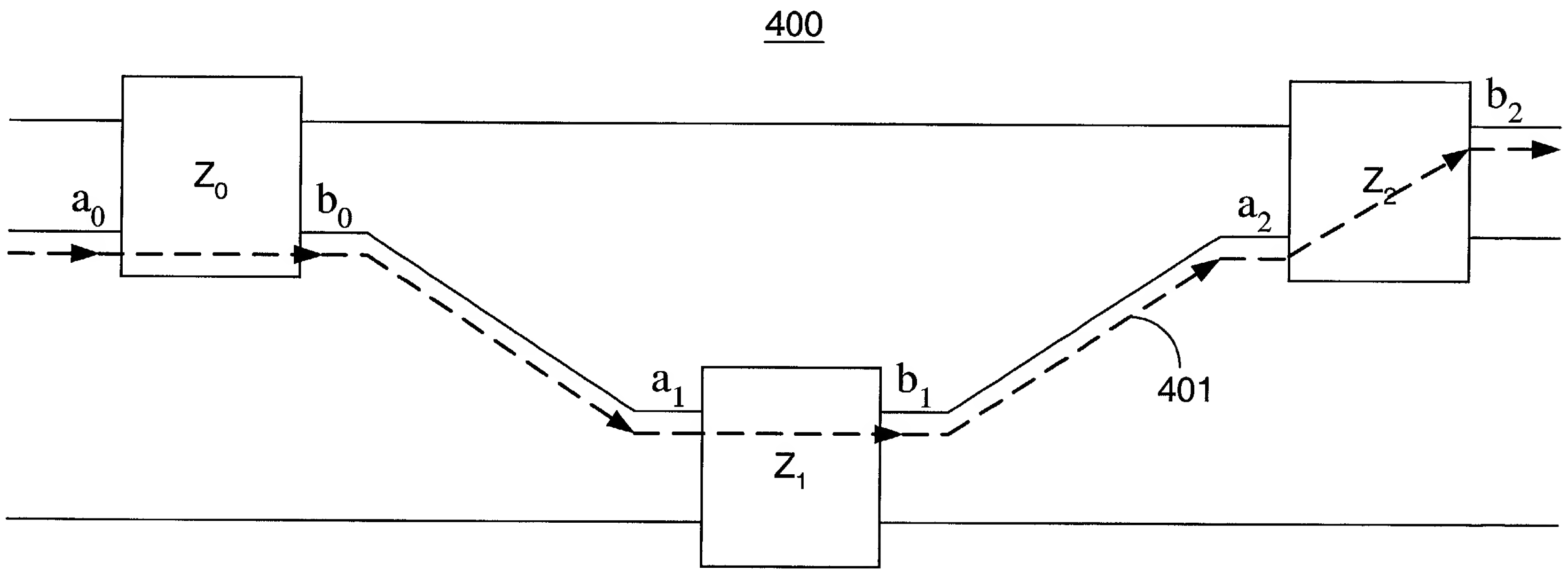


FIG. 4

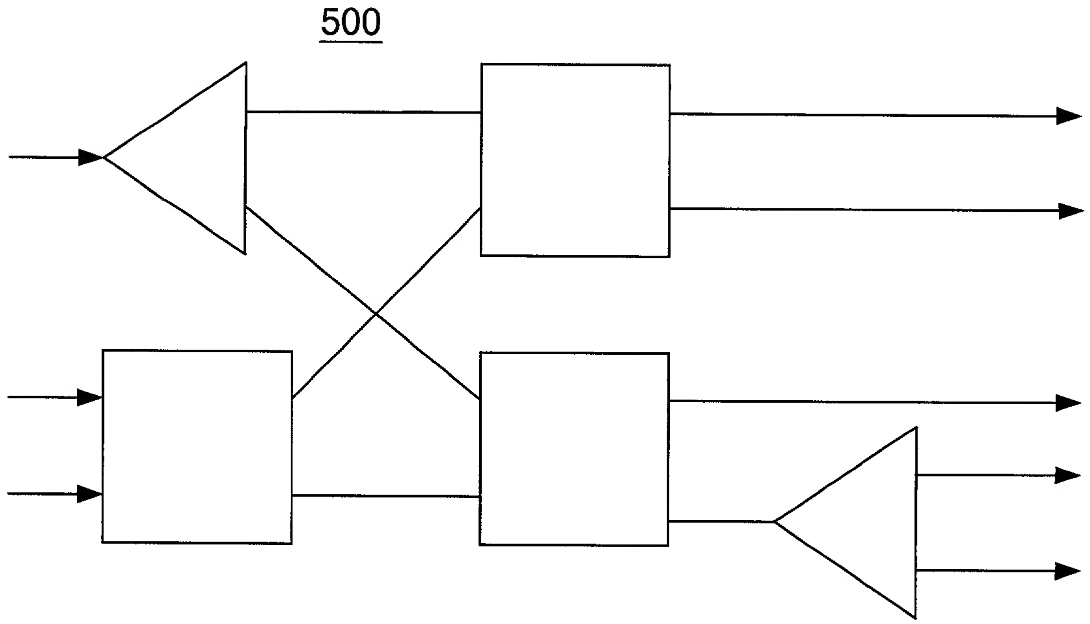


FIG. 5A

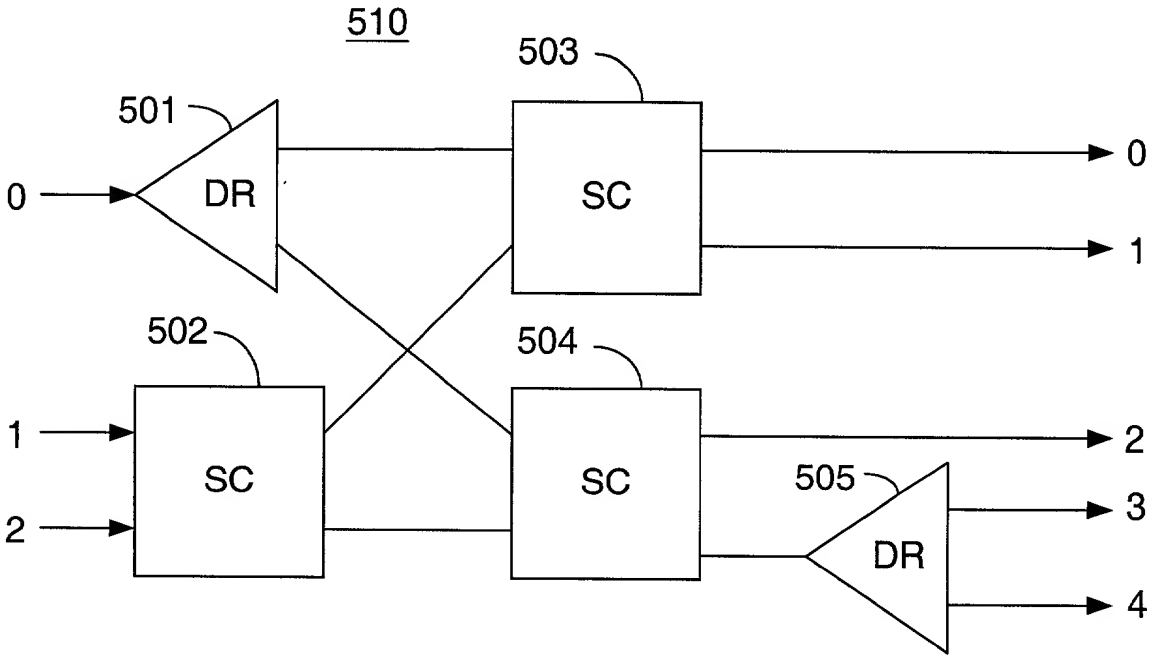


FIG. 5B

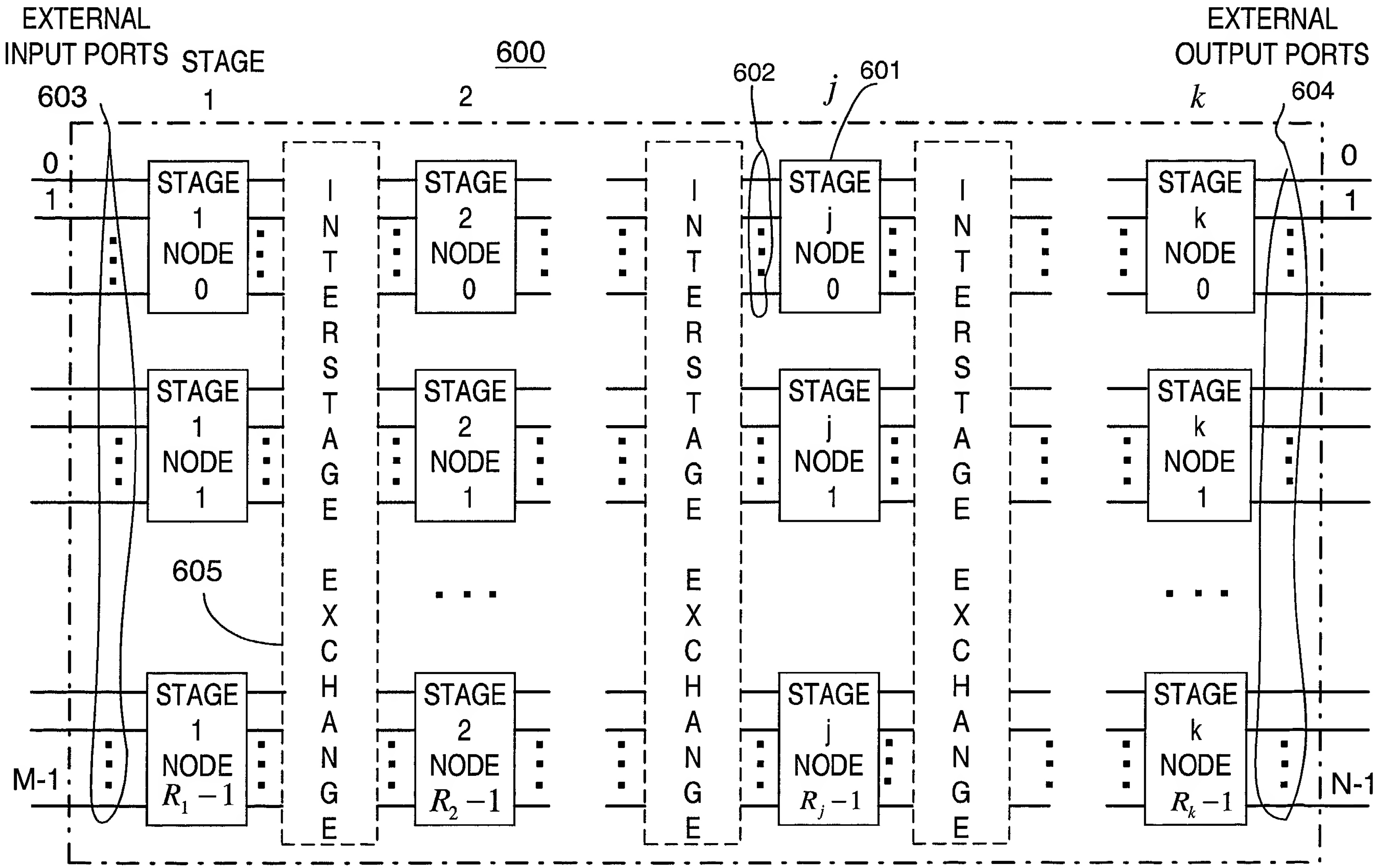

EXTERNAL INPUT PORTS
STAGE
600
EXTERNAL OUTPUT PORTS
603
1
2
602
j
601
k
604
0
1
M-1
0
1
N-1
STAGE 1 NODE 0
STAGE 1 NODE 1
STAGE 1 NODE R_1-1
INTERSTAGE EXCHANGE
STAGE 2 NODE 0
STAGE 2 NODE 1
STAGE 2 NODE R_2-1
INTERSTAGE EXCHANGE
STAGE j NODE 0
STAGE j NODE 1
STAGE j NODE R_j-1
INTERSTAGE EXCHANGE
STAGE k NODE 0
STAGE k NODE 1
STAGE k NODE R_k-1
605

FIG. 6A

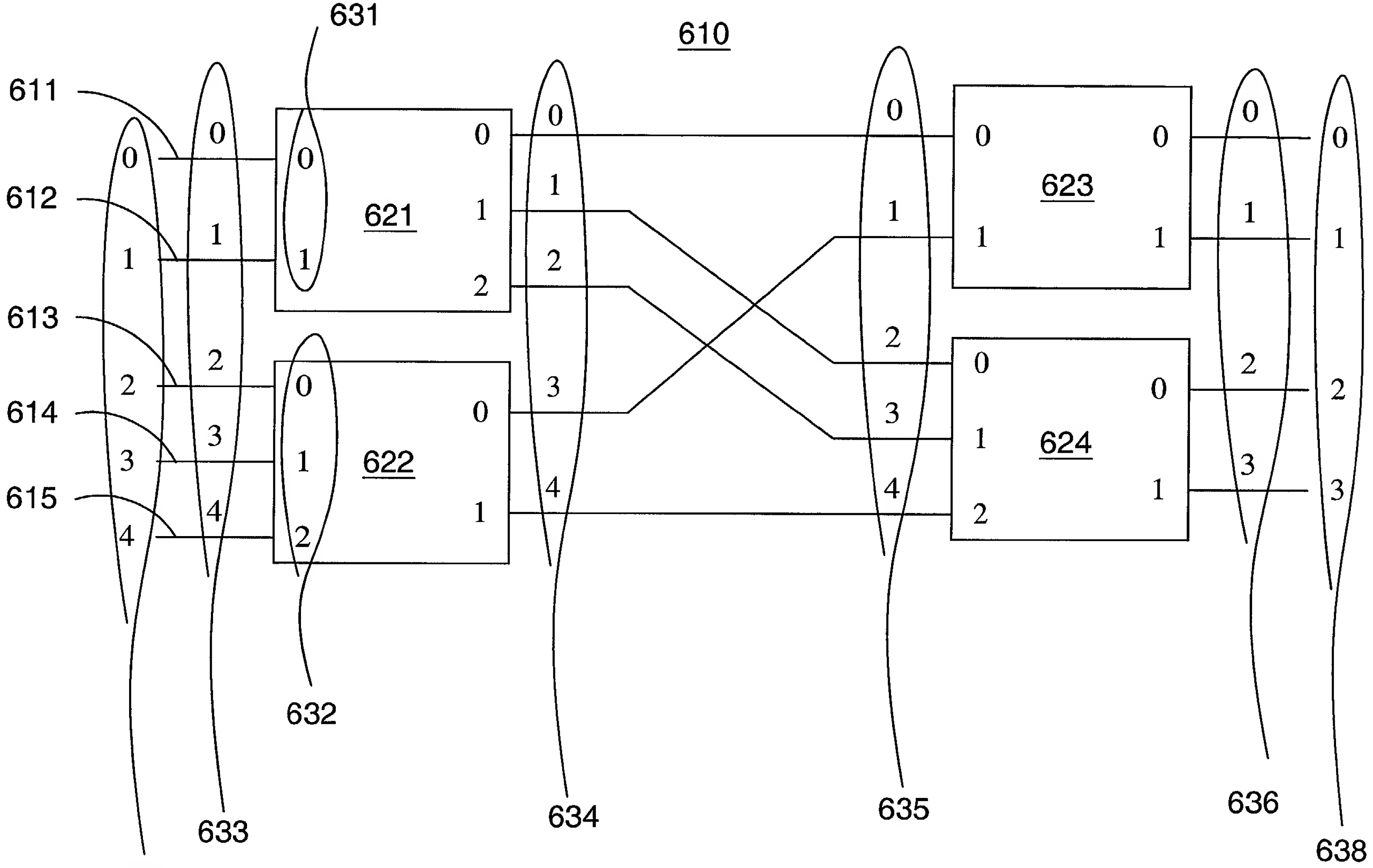

610
611
612
613
614
615
621
622
623
624
631
632
633
634
635
636
637
638
0
1
2
3
4

FIG. 6B

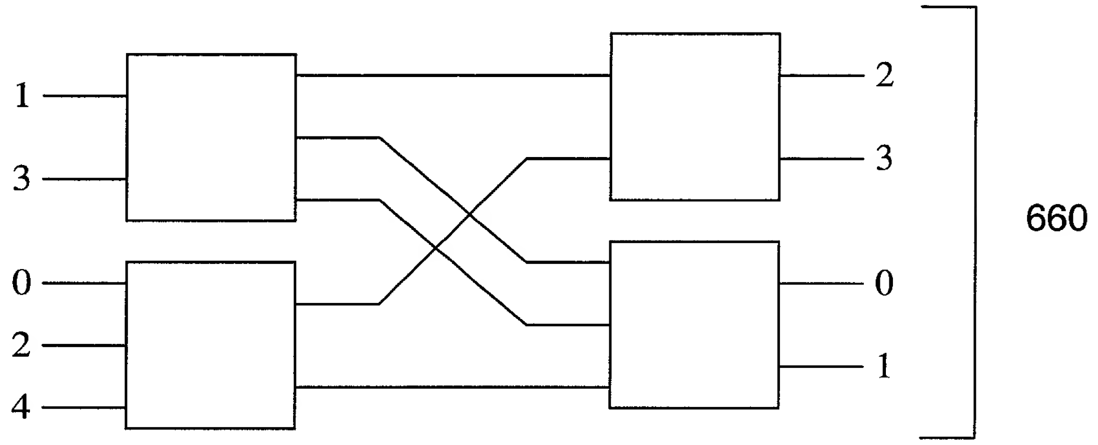

1
3
0
2
4
2
3
0
1
660

FIG. 6C

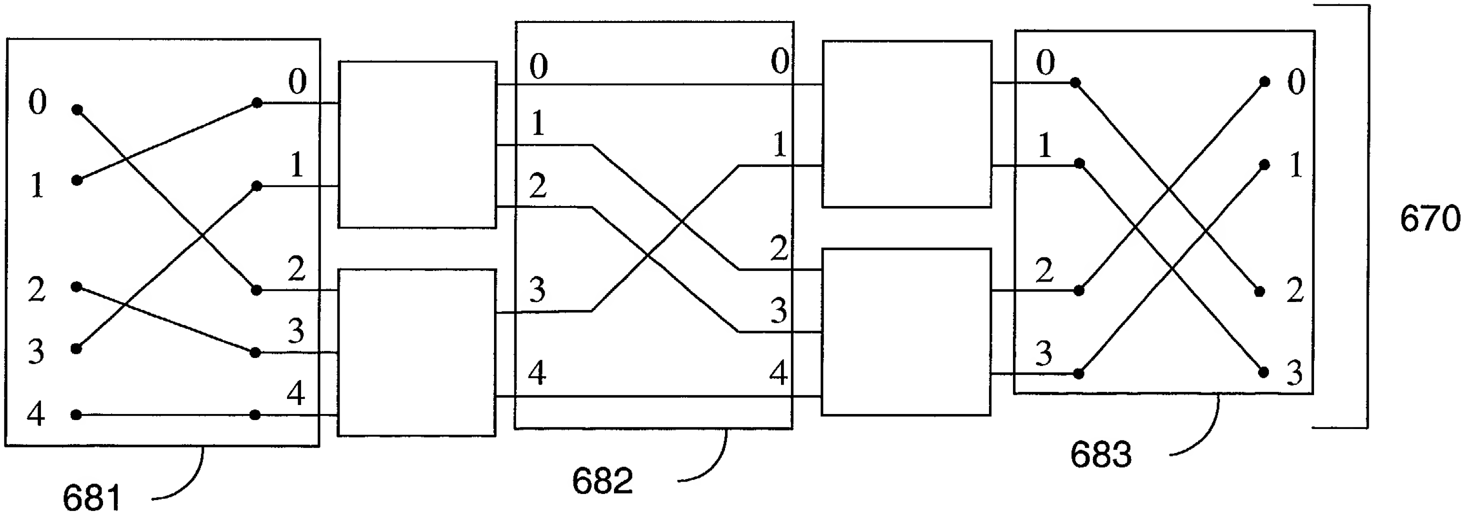

0
1
2
3
4
0
1
2
3
4
0
1
2
3
4
0
1
2
3
4
0
1
2
3
0
1
2
3
681
682
683
670

FIG. 6D

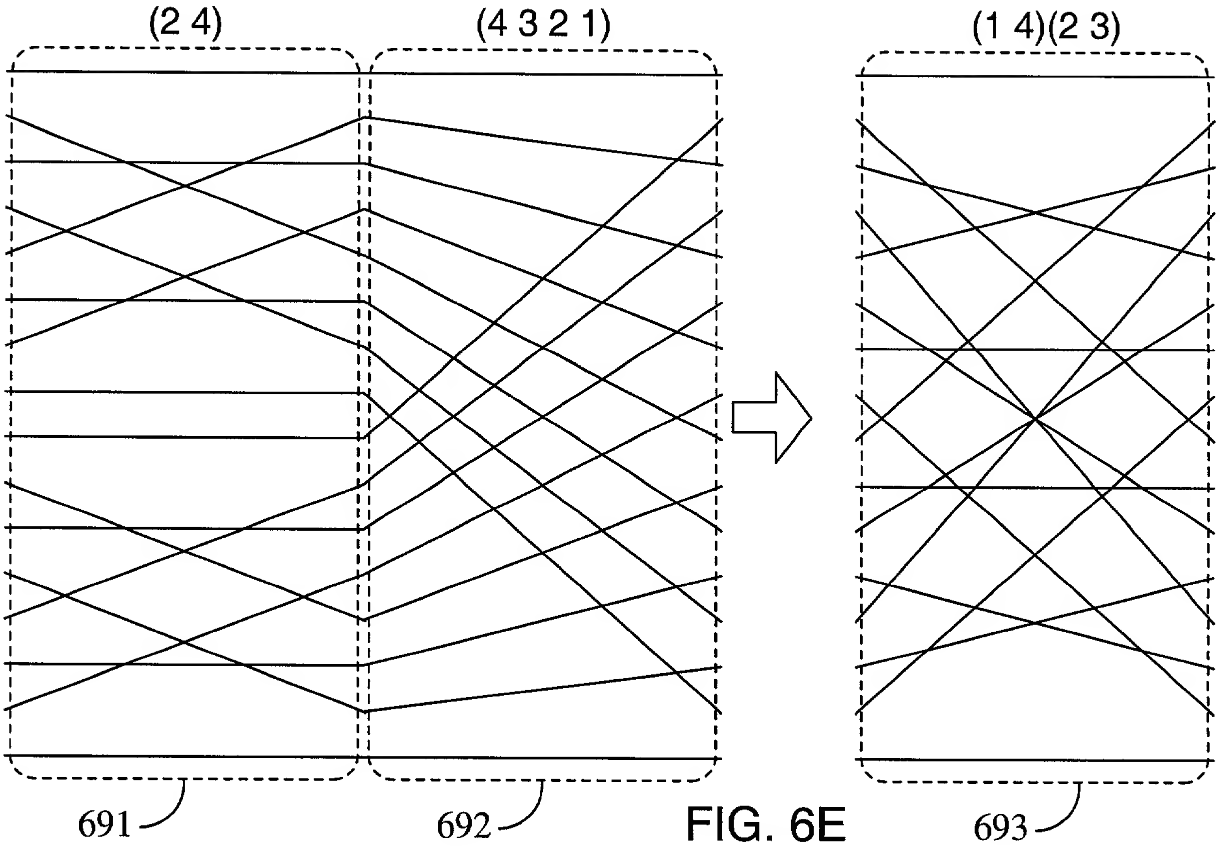


FIG. 6E

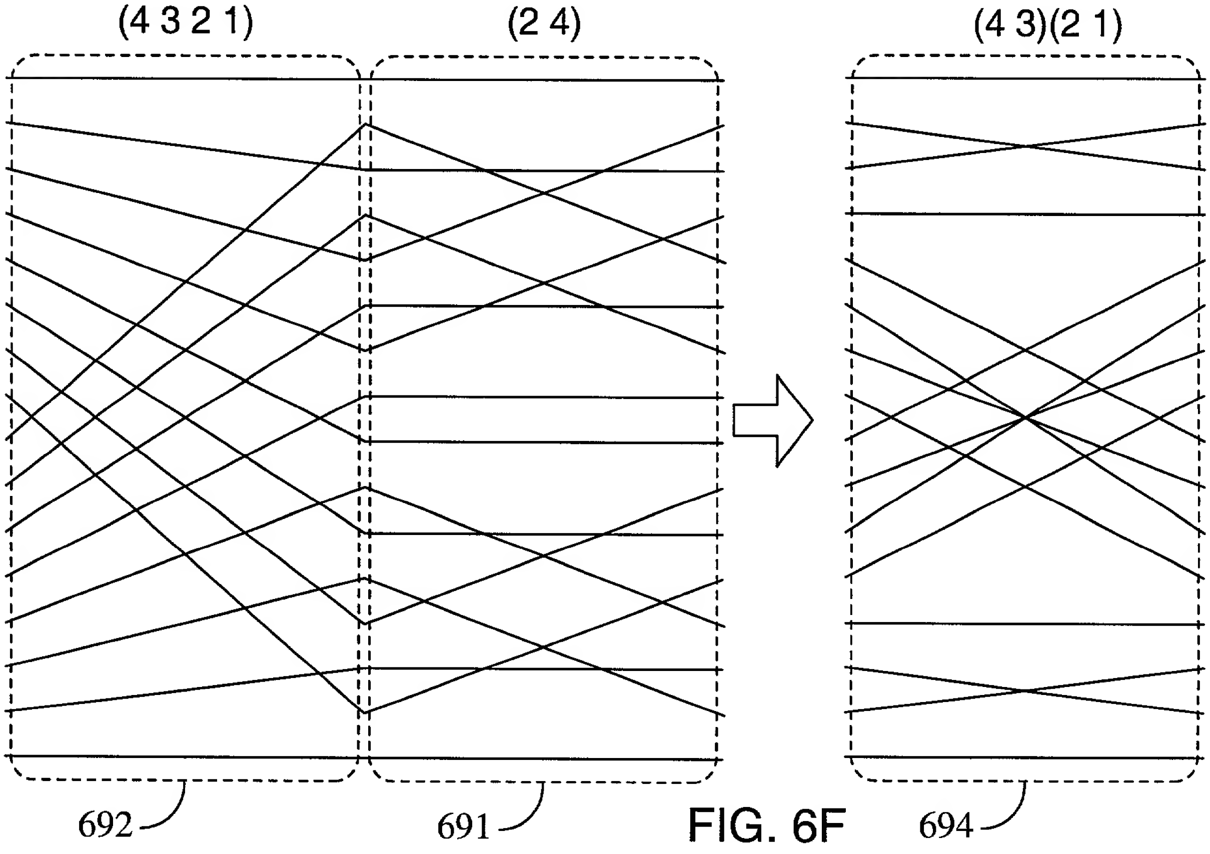


FIG. 6F

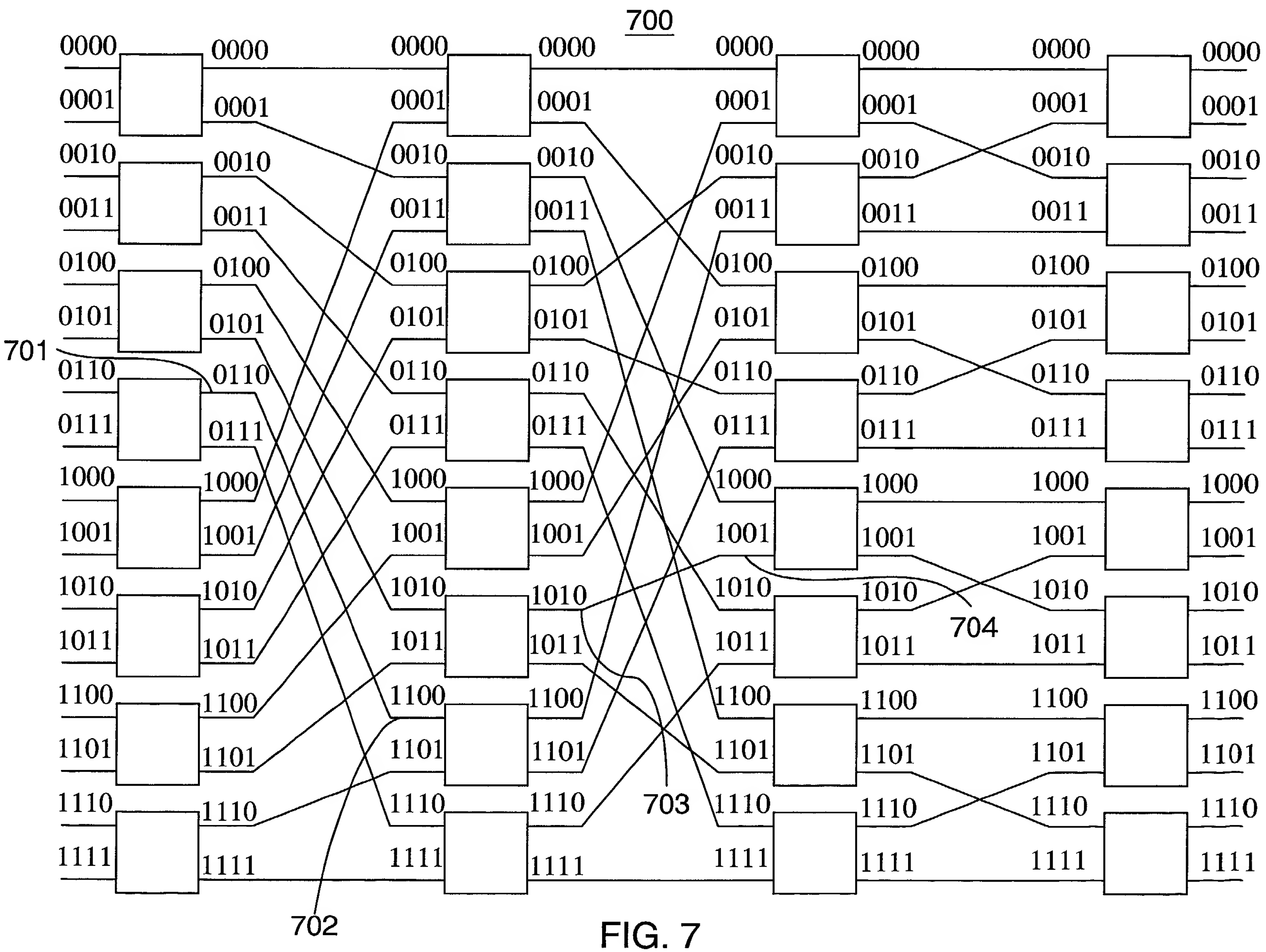

700
701
702
703
704
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

FIG. 7

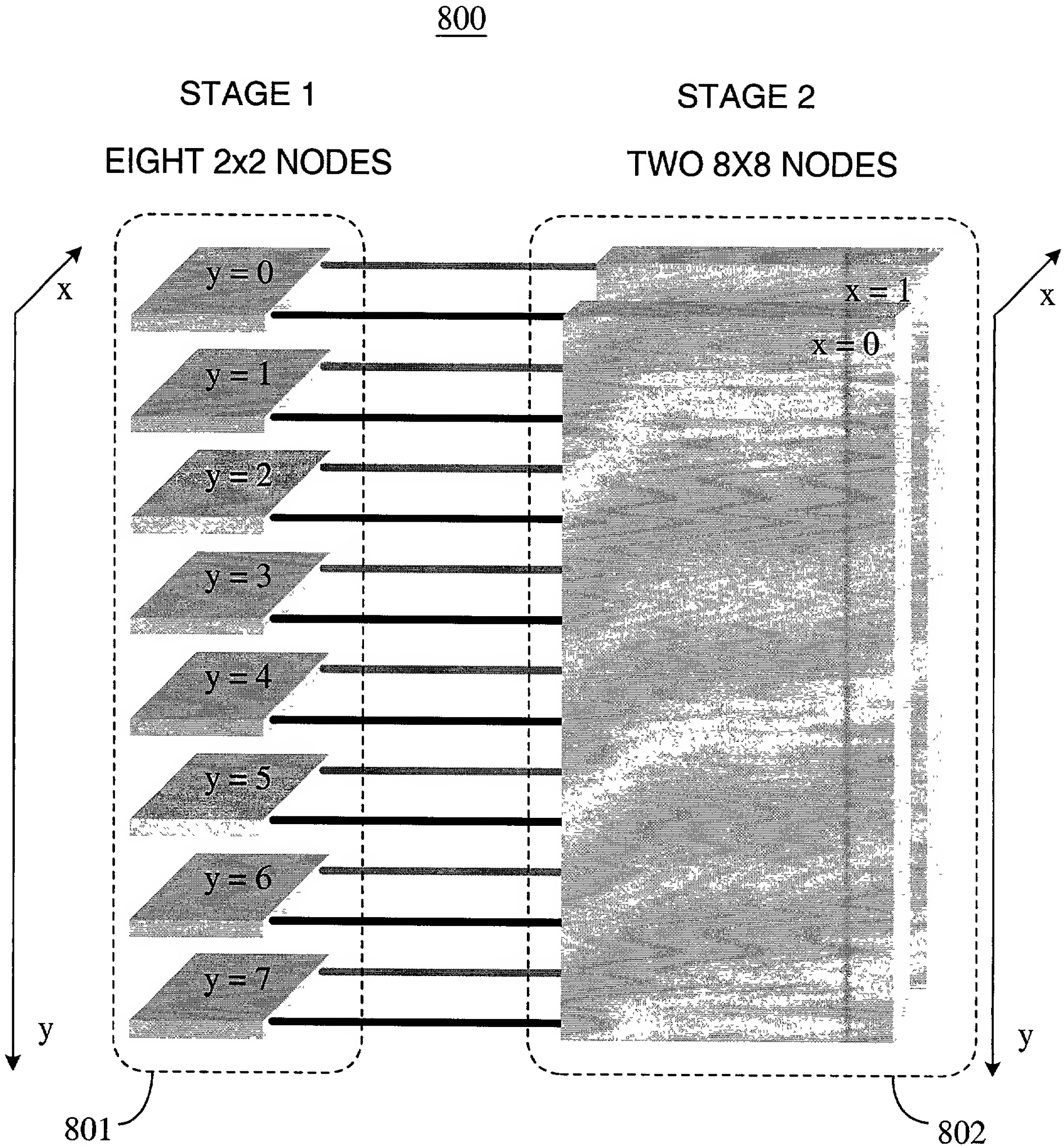

800
STAGE 1
EIGHT 2x2 NODES
STAGE 2
TWO 8X8 NODES
x
y = 0
y = 1
y = 2
y = 3
y = 4
y = 5
y = 6
y = 7
y
x = 1
x = 0
x
y
801
802

FIG. 8

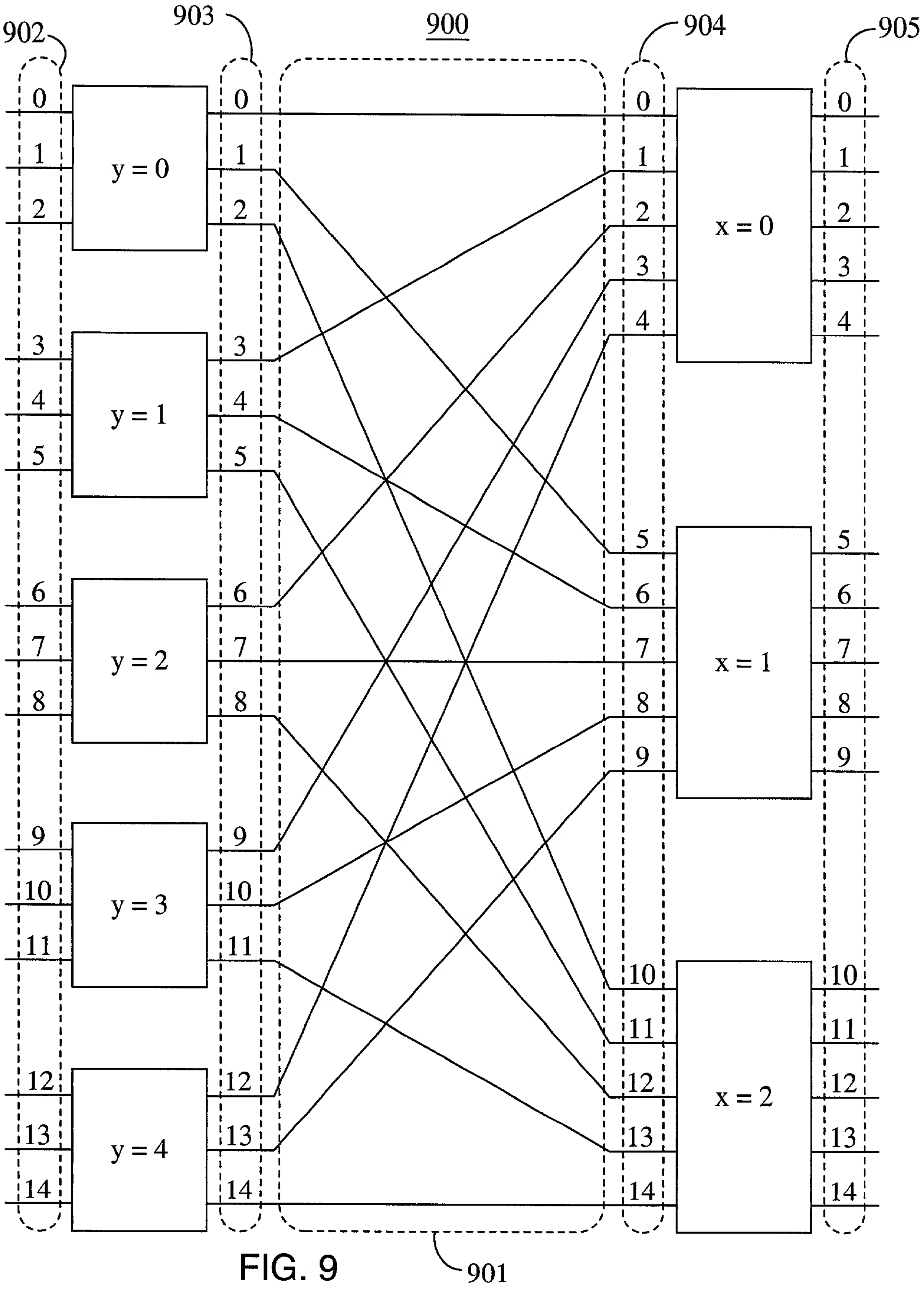

902
903
900
904
905
y = 0
y = 1
y = 2
y = 3
y = 4
x = 0
x = 1
x = 2
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
901

FIG. 9

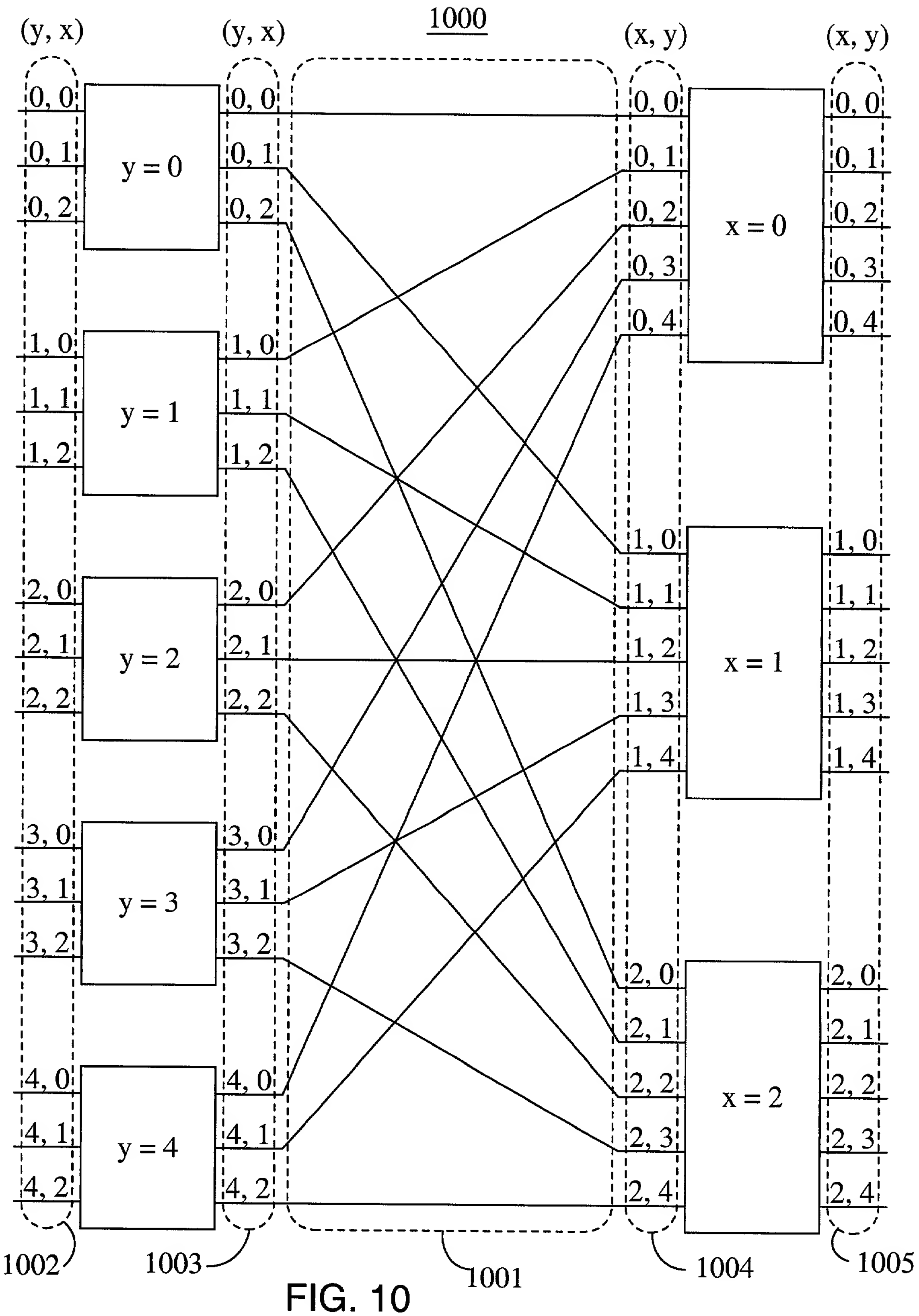

1000
(y, x)
(y, x)
(x, y)
(x, y)
0, 0
0, 1
0, 2
1, 0
1, 1
1, 2
2, 0
2, 1
2, 2
3, 0
3, 1
3, 2
4, 0
4, 1
4, 2
y = 0
y = 1
y = 2
y = 3
y = 4
0, 0
0, 1
0, 2
0, 3
0, 4
1, 0
1, 1
1, 2
1, 3
1, 4
2, 0
2, 1
2, 2
2, 3
2, 4
x = 0
x = 1
x = 2
1002
1003
1001
1004
1005

FIG. 10

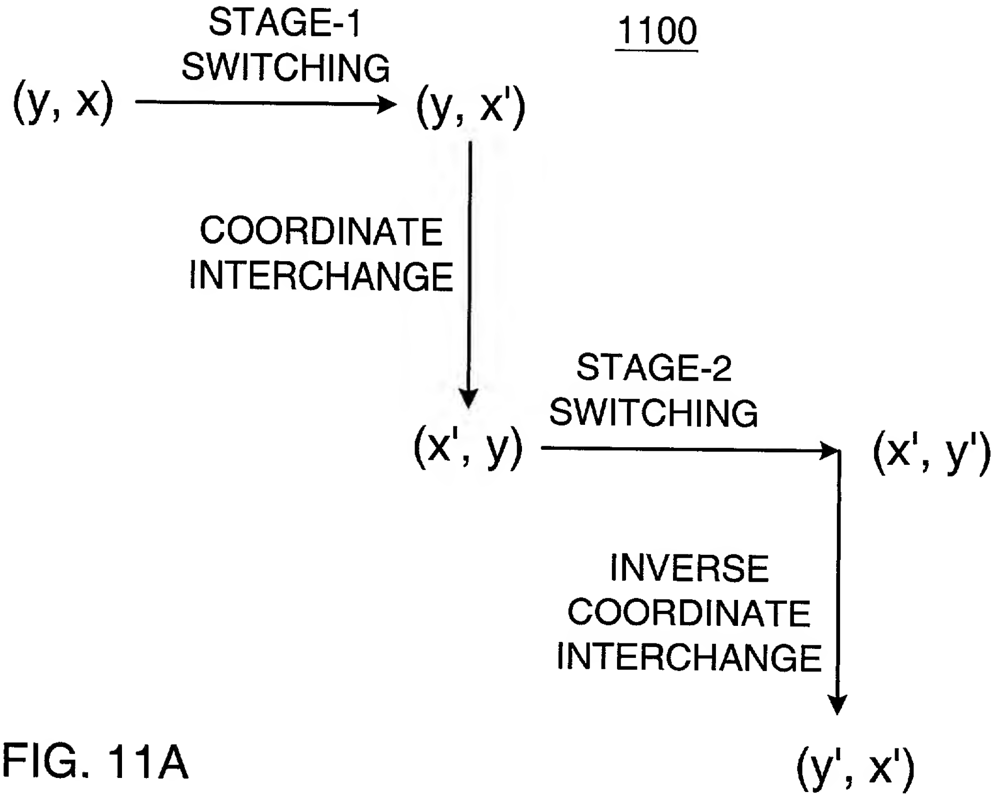


FIG. 11A

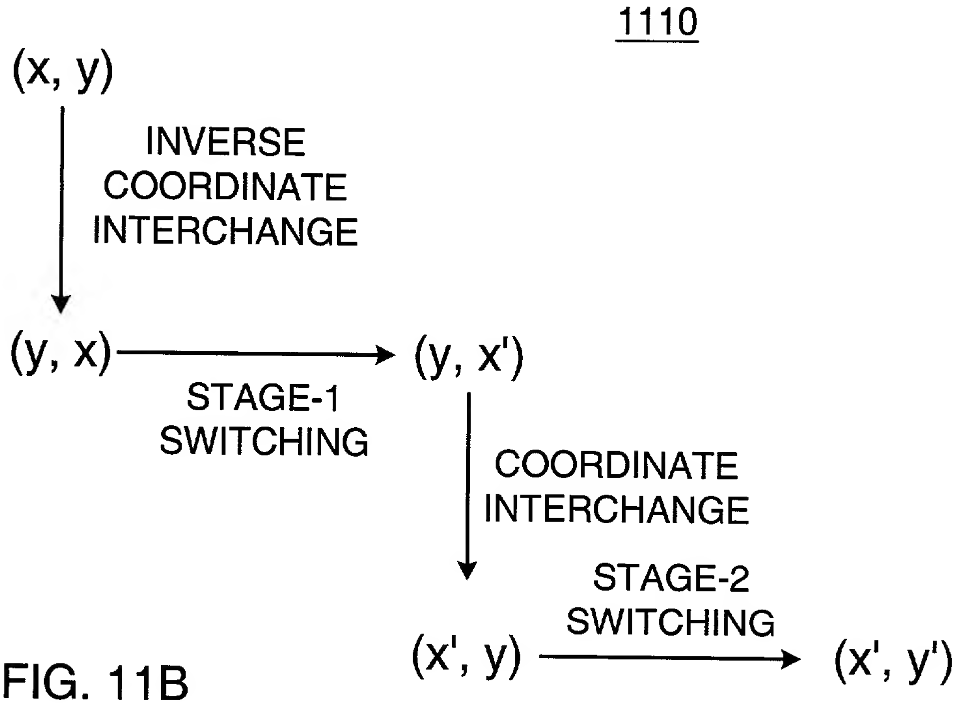


FIG. 11B

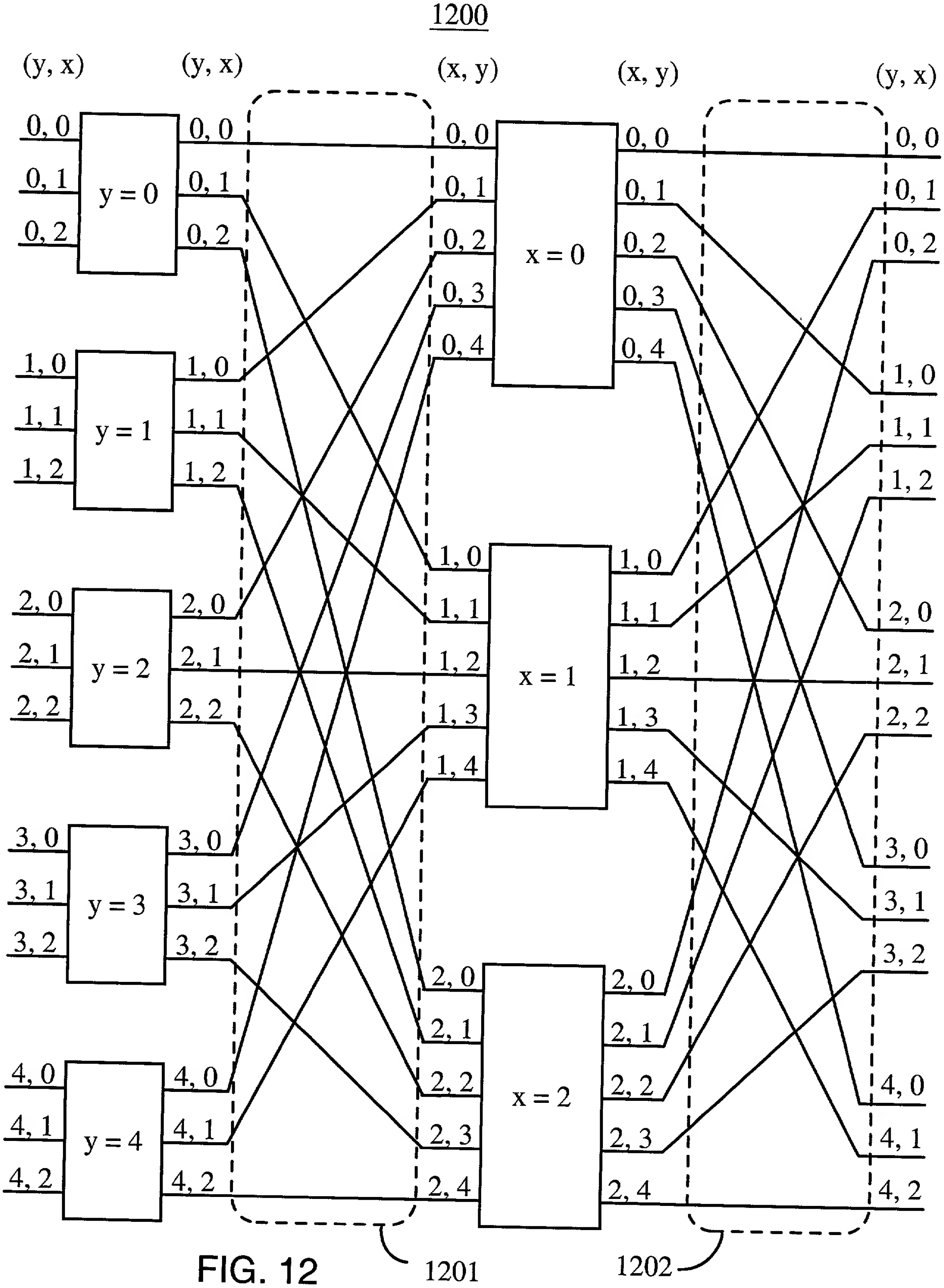

1200
(y, x)
(y, x)
(x, y)
(x, y)
(y, x)
0, 0
0, 1
0, 2
y = 0
1, 0
1, 1
1, 2
y = 1
2, 0
2, 1
2, 2
y = 2
3, 0
3, 1
3, 2
y = 3
4, 0
4, 1
4, 2
y = 4
0, 0
0, 1
0, 2
0, 3
0, 4
x = 0
1, 0
1, 1
1, 2
1, 3
1, 4
x = 1
2, 0
2, 1
2, 2
2, 3
2, 4
x = 2
1201
1202

FIG. 12

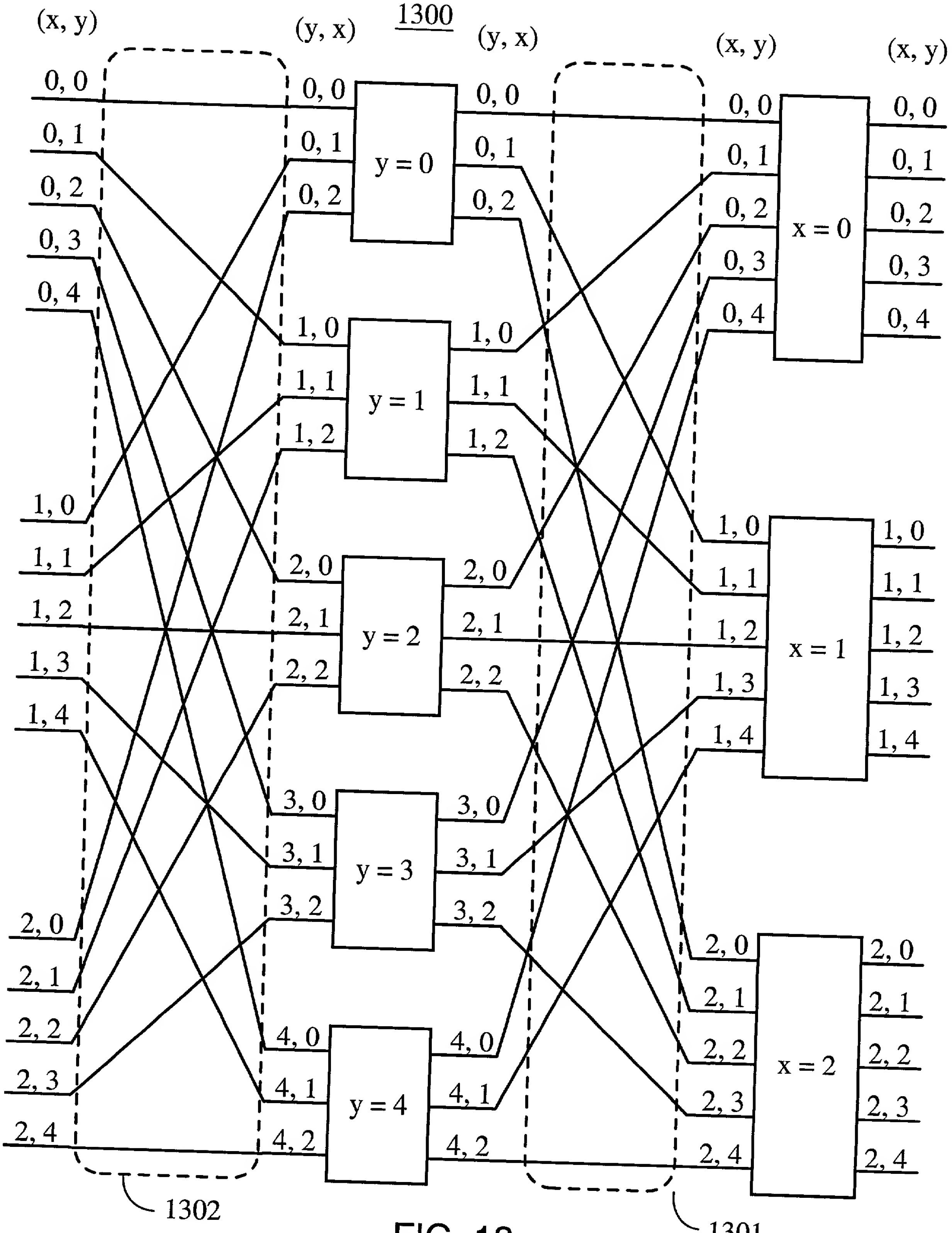
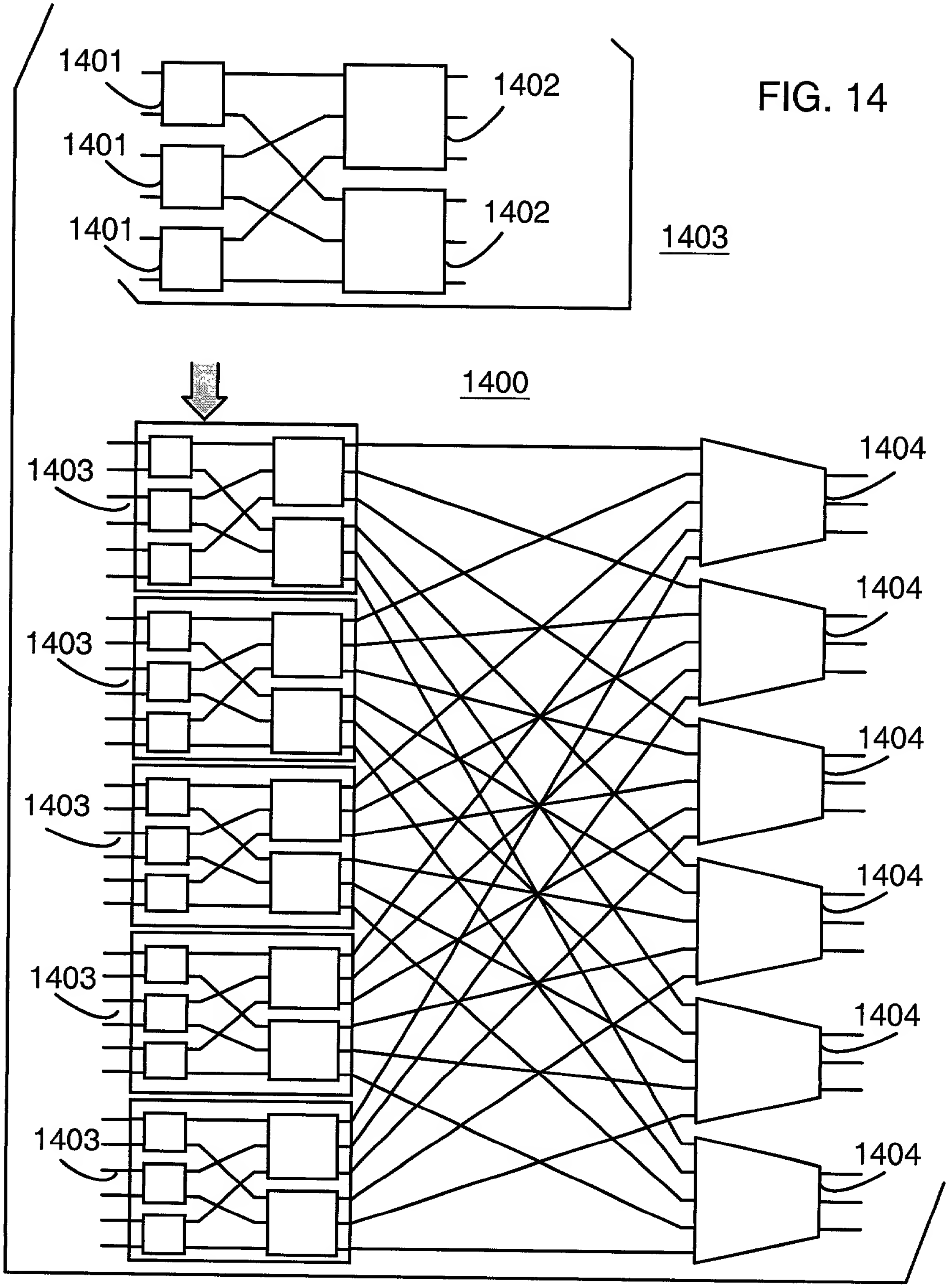

1300
(x, y)
(y, x)
(y, x)
(x, y)
(x, y)
0, 0
0, 1
0, 2
0, 3
0, 4
1, 0
1, 1
1, 2
1, 3
1, 4
2, 0
2, 1
2, 2
2, 3
2, 4
y = 0
y = 1
y = 2
y = 3
y = 4
3, 0
3, 1
3, 2
4, 0
4, 1
4, 2
x = 0
x = 1
x = 2
1302
1301

FIG. 13

FIG. 14


1401
1401
1401
1402
1402
1403
1400
1403
1403
1403
1403
1403
1404
1404
1404
1404
1404
1404

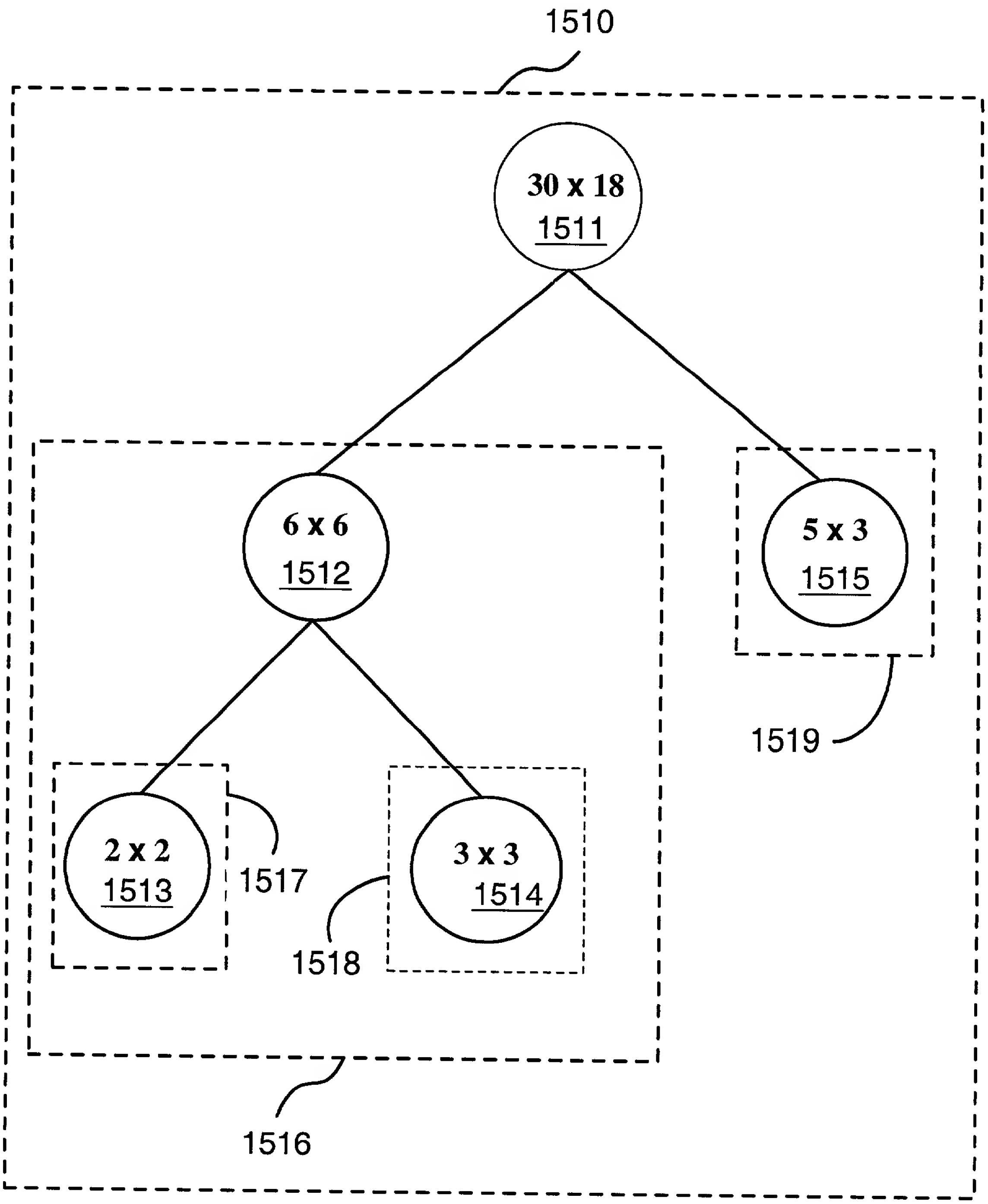

1510
30 x 18
1511
6 x 6
1512
5 x 3
1515
1519
2 x 2
1513
1517
3 x 3
1514
1518
1516

FIG. 15

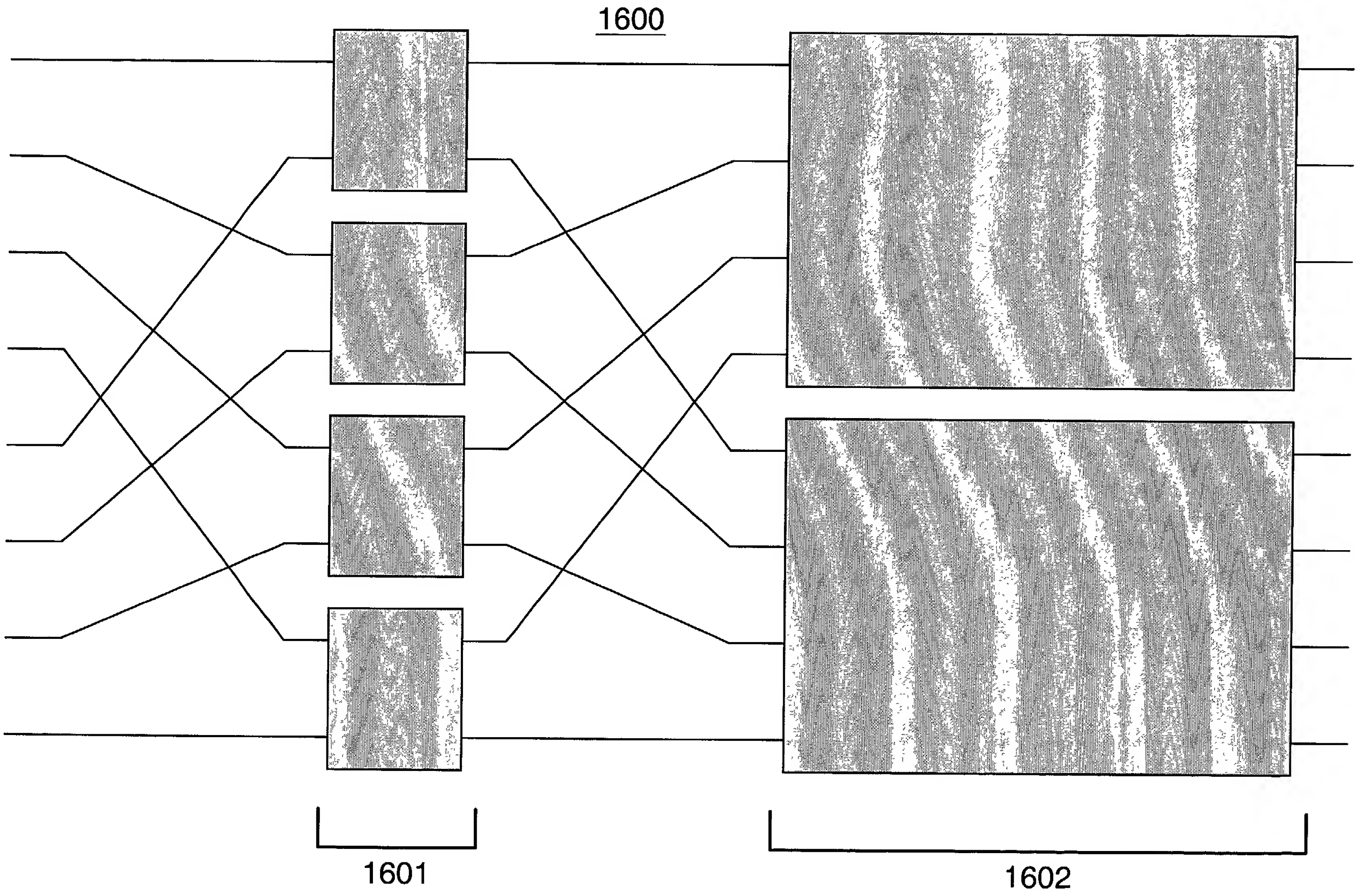


FIG. 16

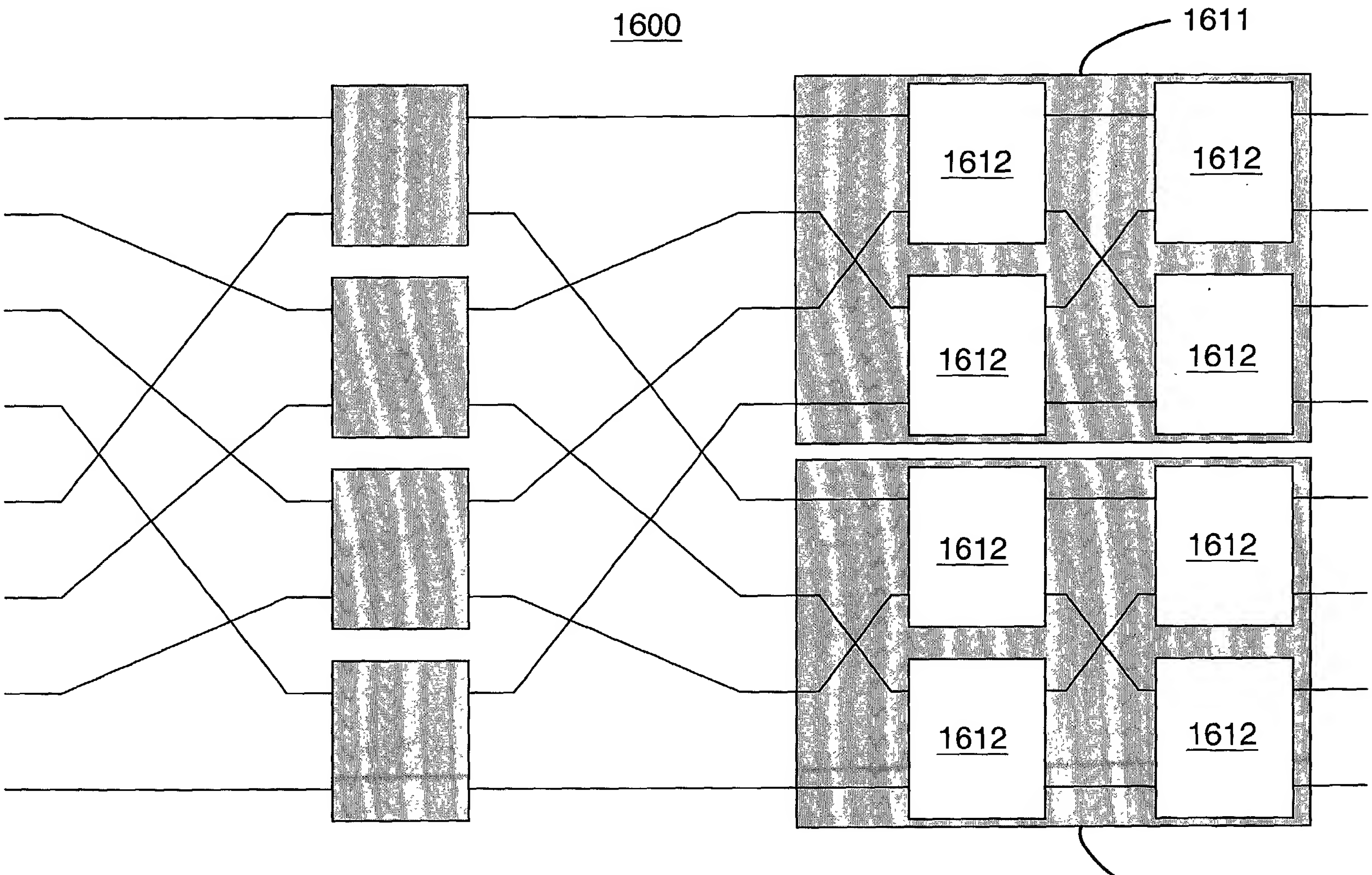


FIG. 17

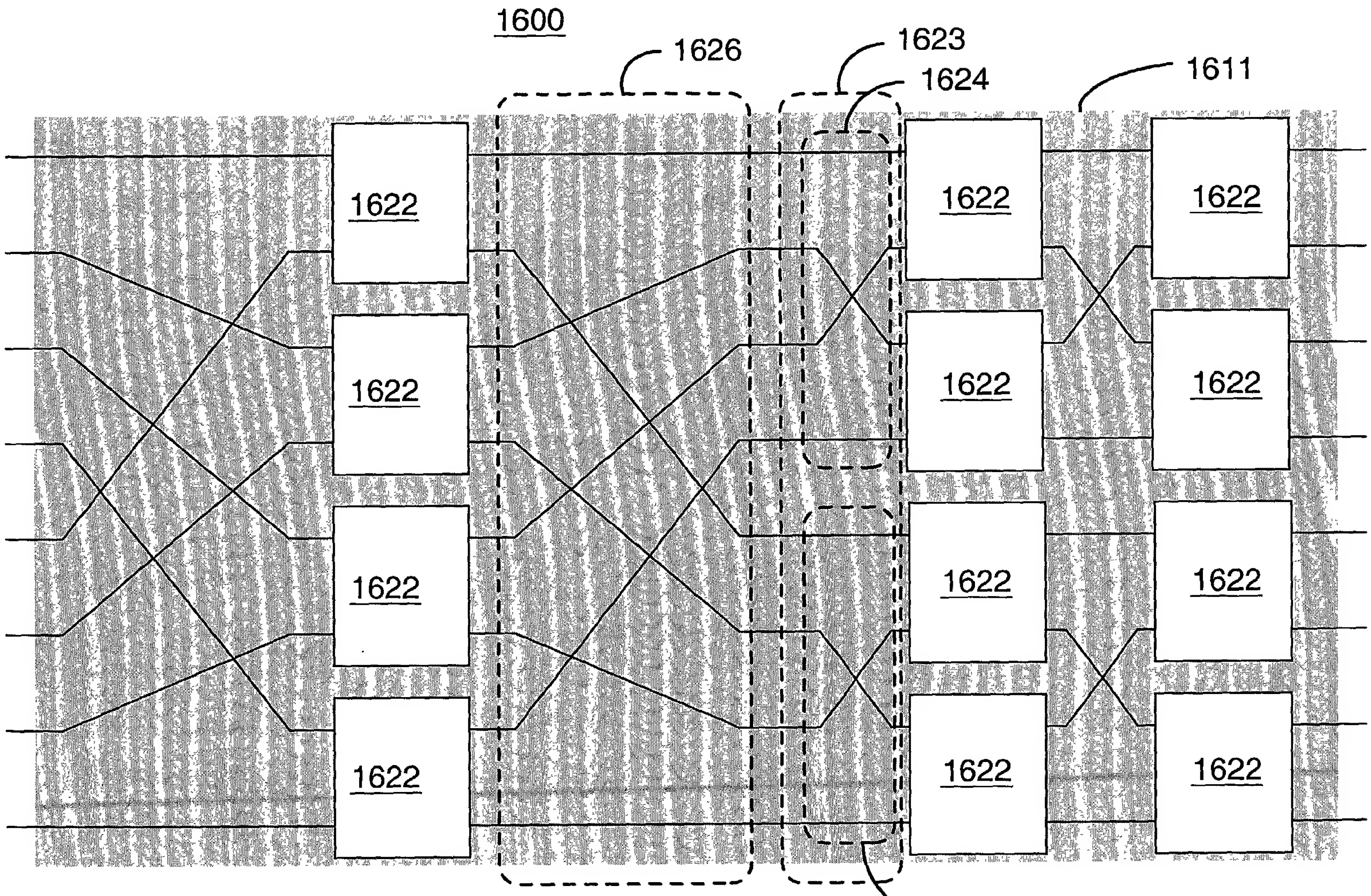

1600
1626
1623
1624
1611
1622
1622
1622
1622
1622
1622
1622
1622
1622
1622
1622
1622
1625

FIG. 18

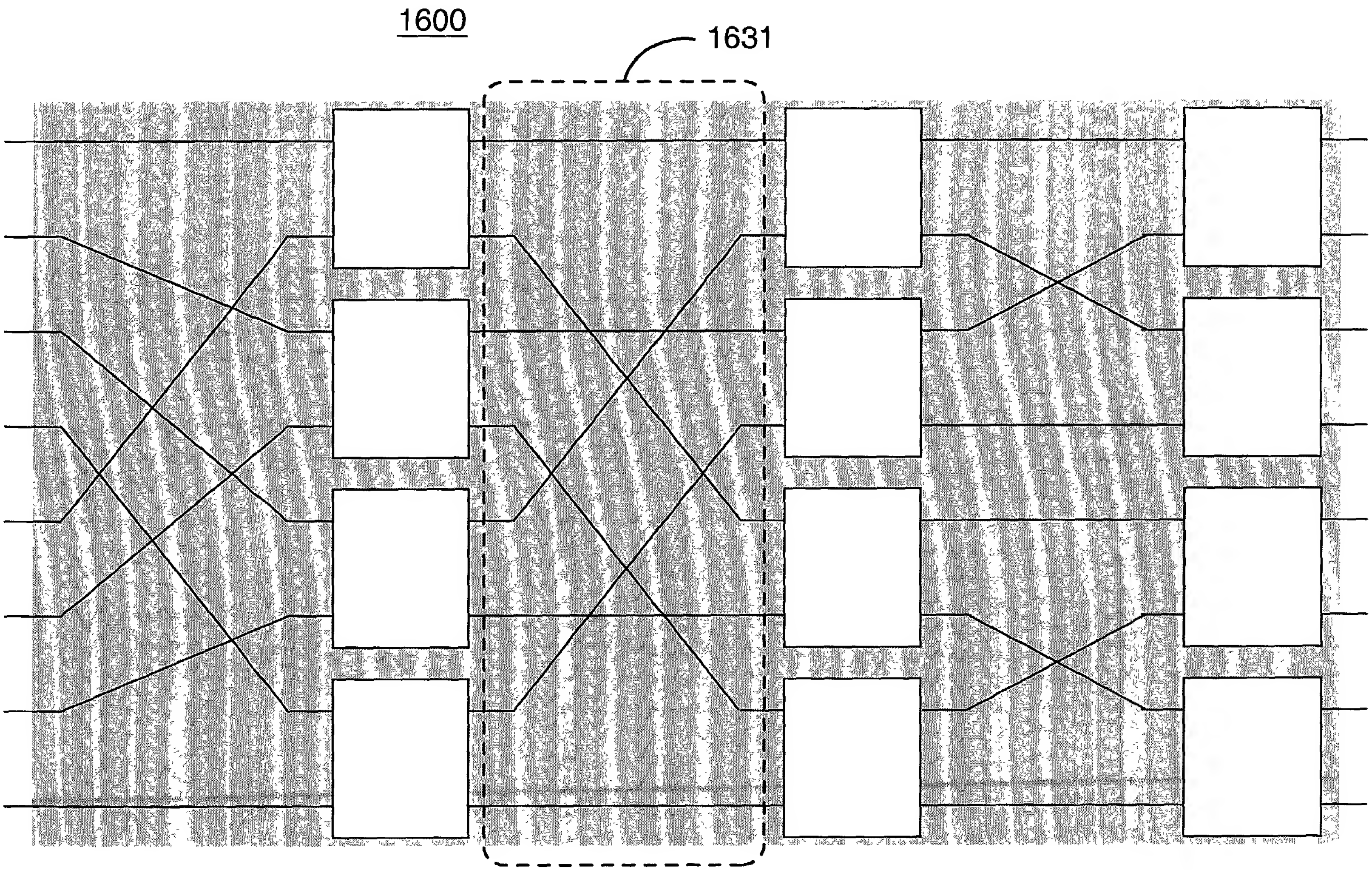


FIG. 19

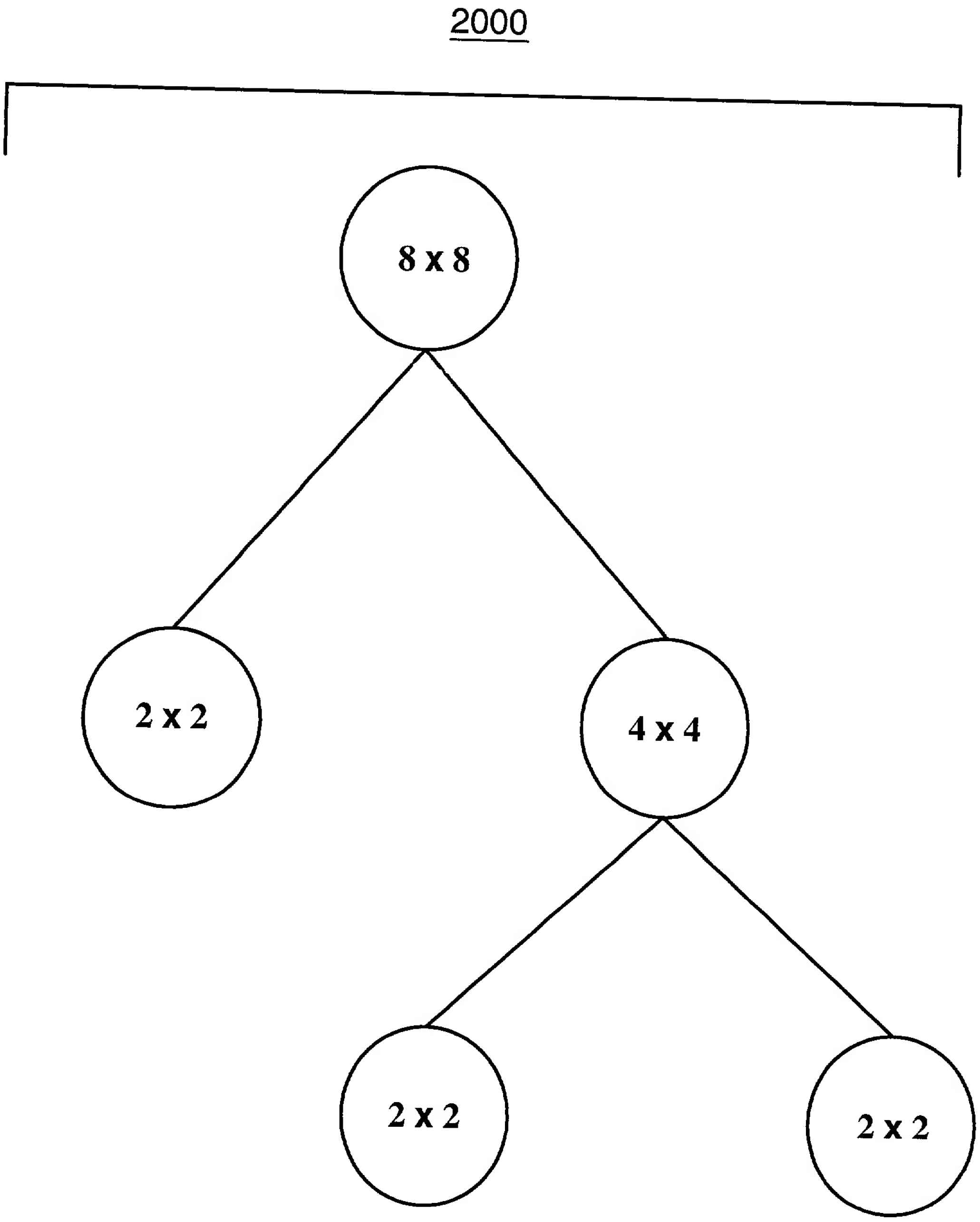


FIG. 20

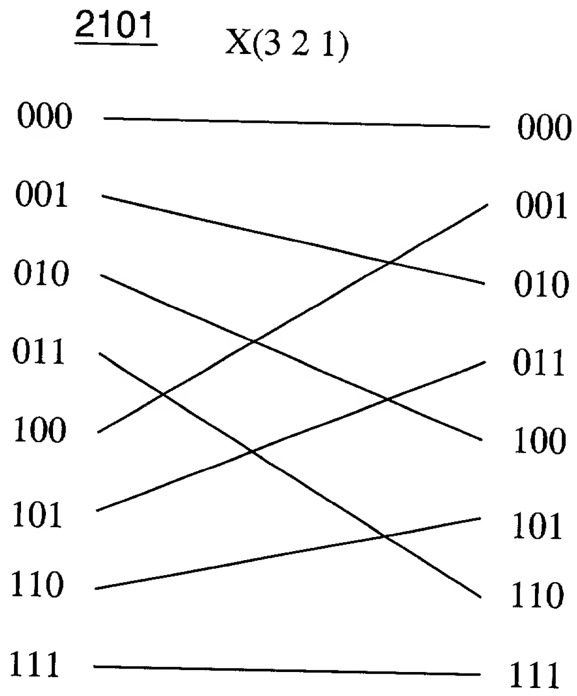


FIG. 21A

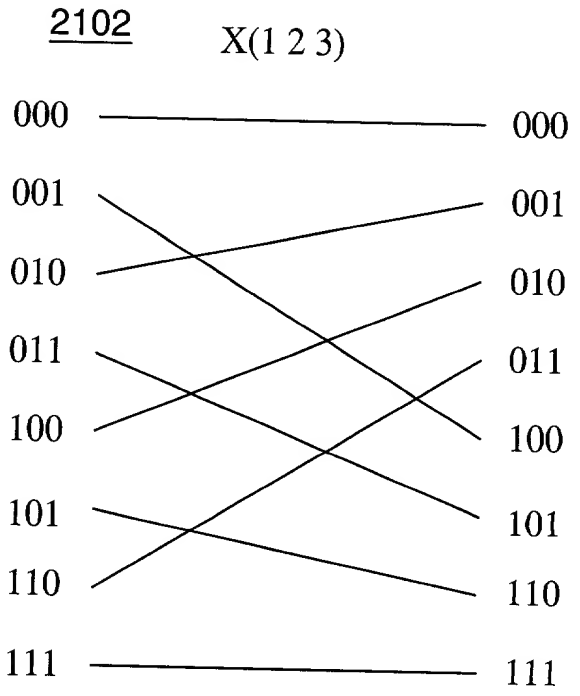


FIG. 21B

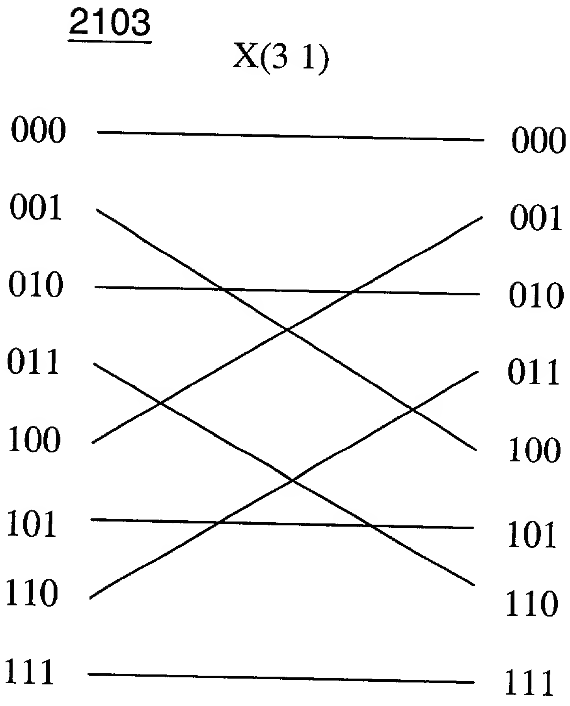


FIG. 21C

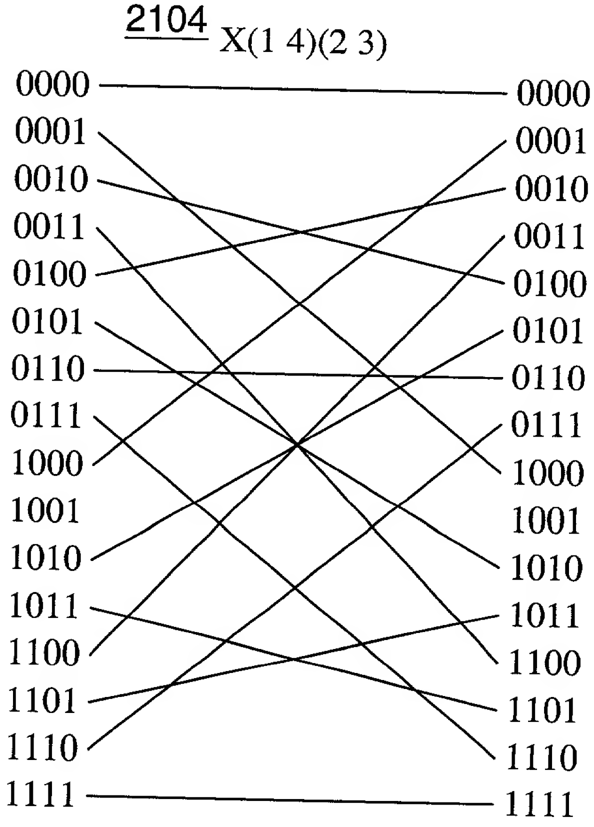
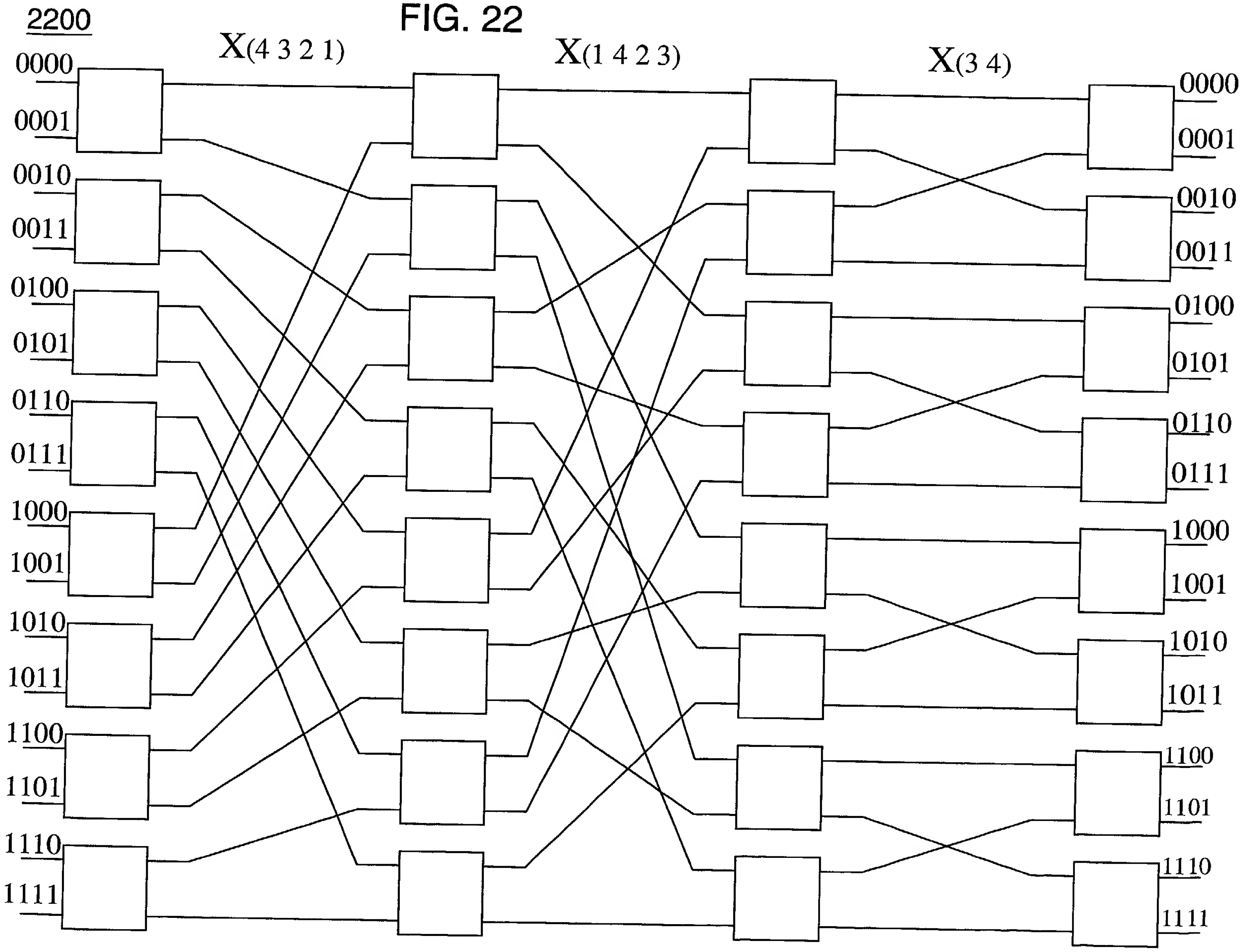


FIG. 21D

FIG. 22


2200
X(4 3 2 1)
X(1 4 2 3)
X(3 4)
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

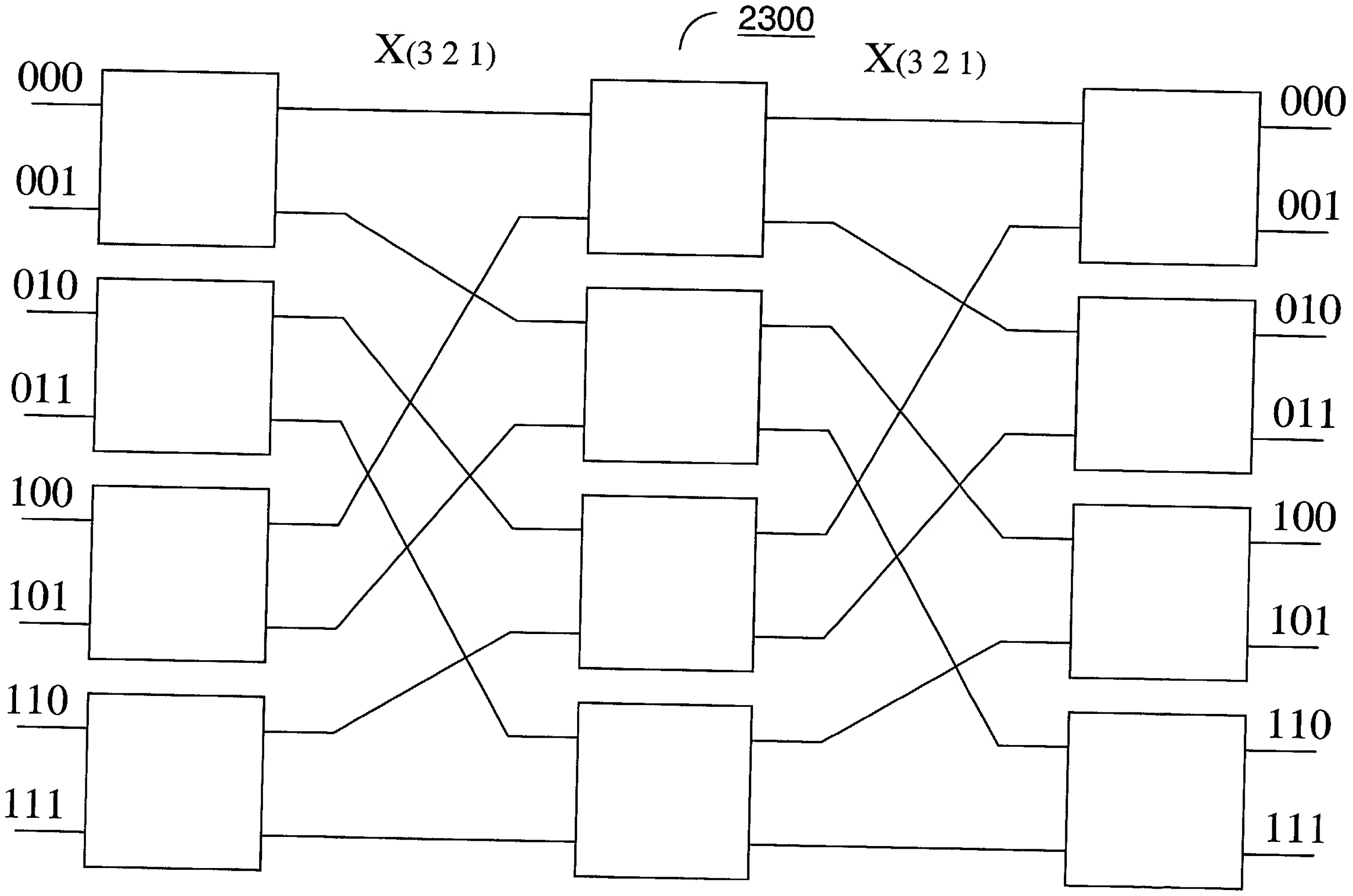
2300
X(3 2 1)
X(3 2 1)
000
001
010
011
100
101
110
111
000
001
010
011
100
101
110
111

FIG. 23

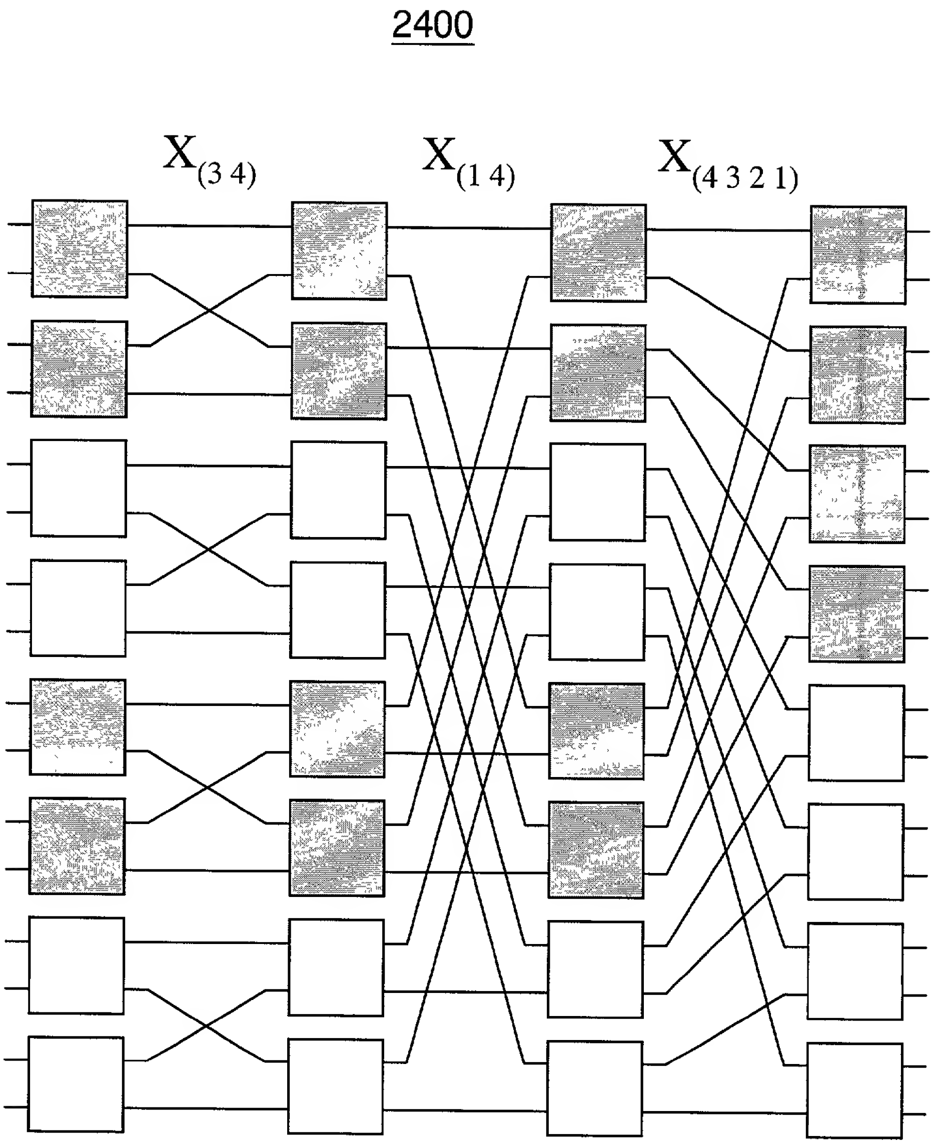


FIG. 24

FIG. 25

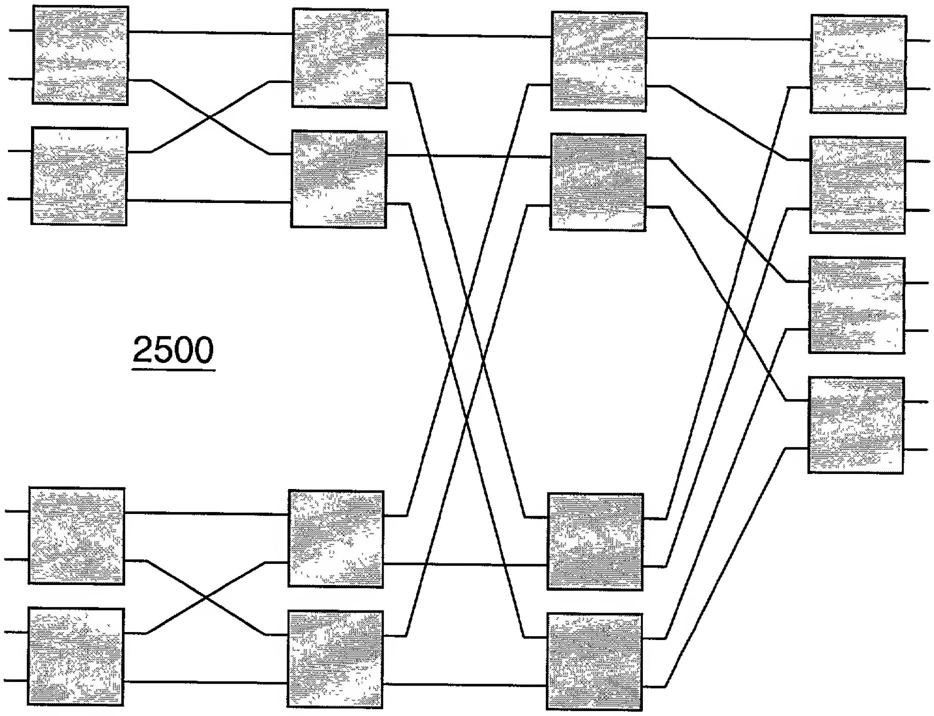
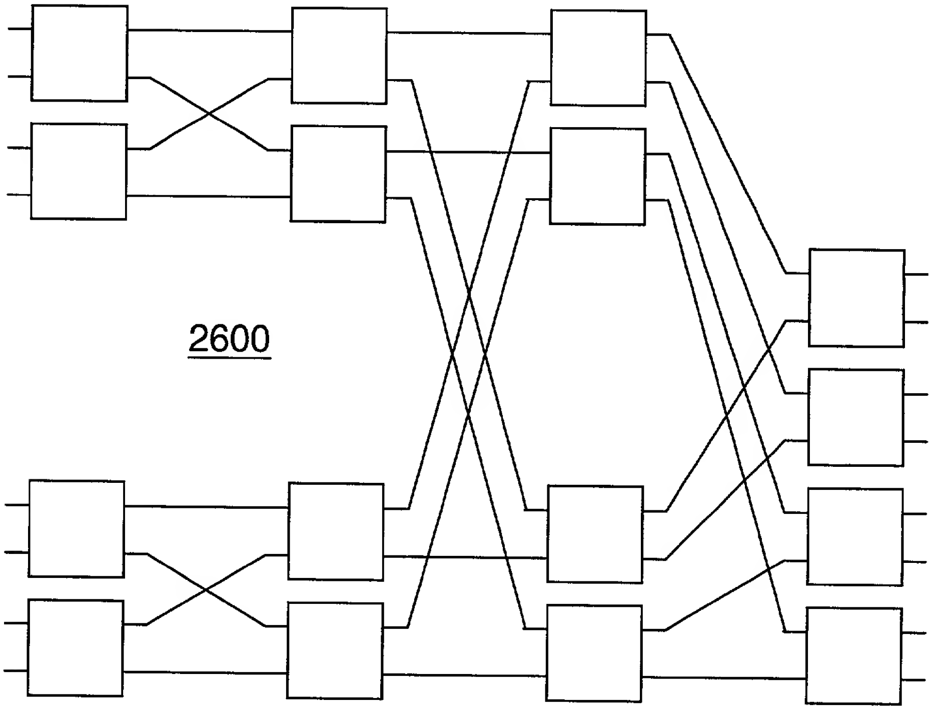


FIG. 26



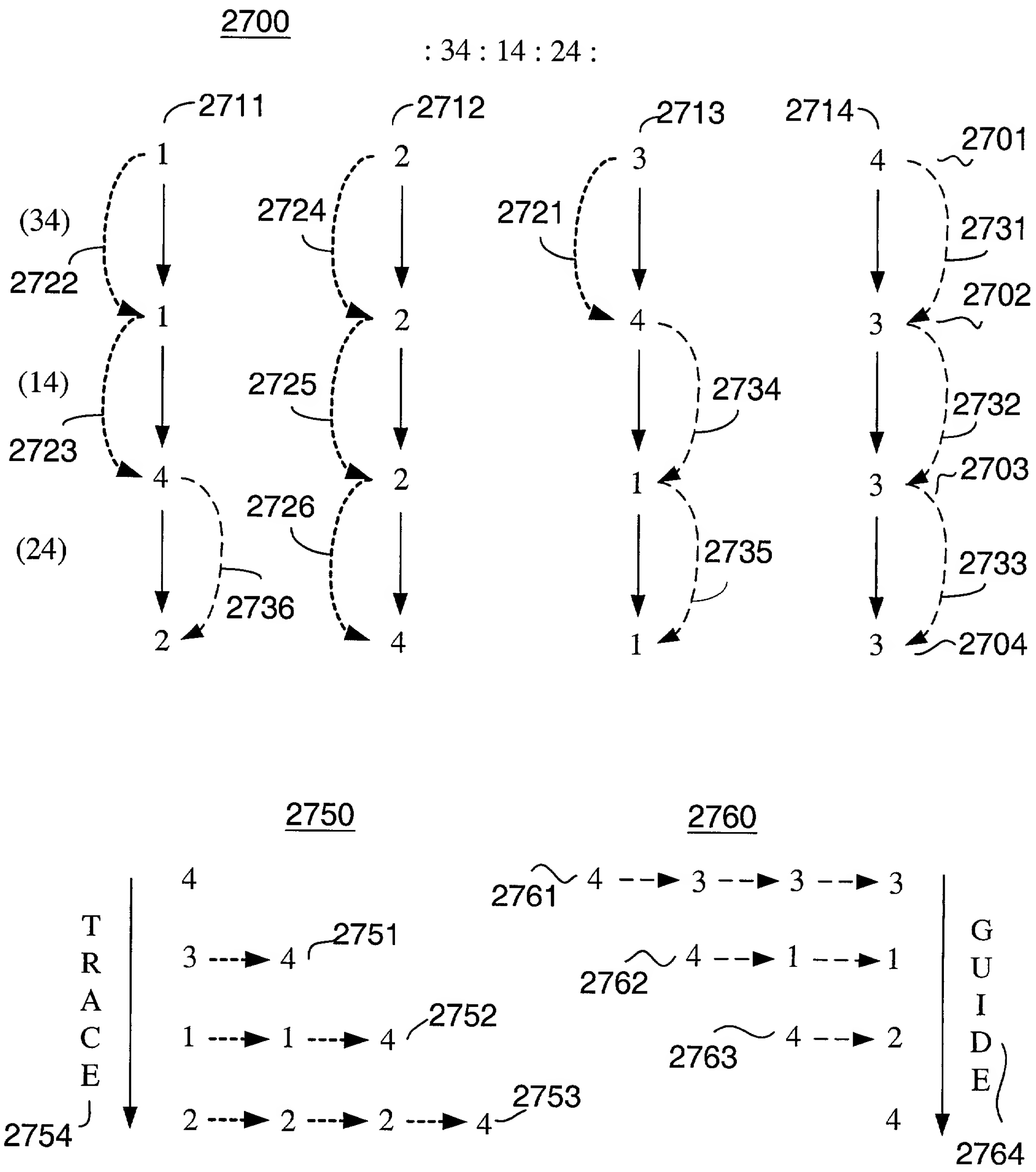

2700
: 34 : 14 : 24 :
2711
2712
2713
2714
2701
2702
2703
2704
2721
2722
2723
2724
2725
2726
2731
2732
2733
2734
2735
2736
(34)
(14)
(24)
1 1 4 2
2 2 2 4
3 4 1 1
4 3 3 3
2750
TRACE
2754
4
3 → 4
1 → 1 → 4
2 → 2 → 2 → 4
2751
2752
2753
2760
GUIDE
2764
2761 4 → 3 → 3 → 3
2762 4 → 1 → 1
2763 4 → 2
4

FIG. 27

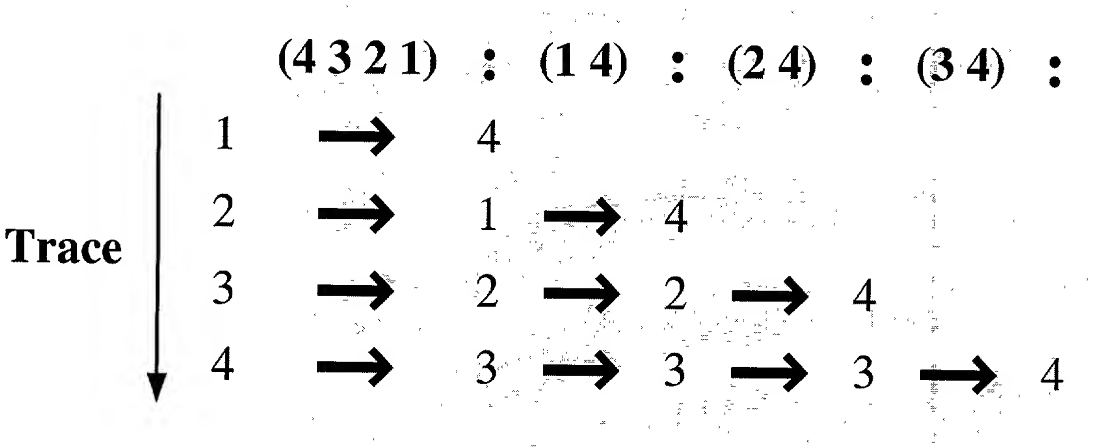


FIG. 28A

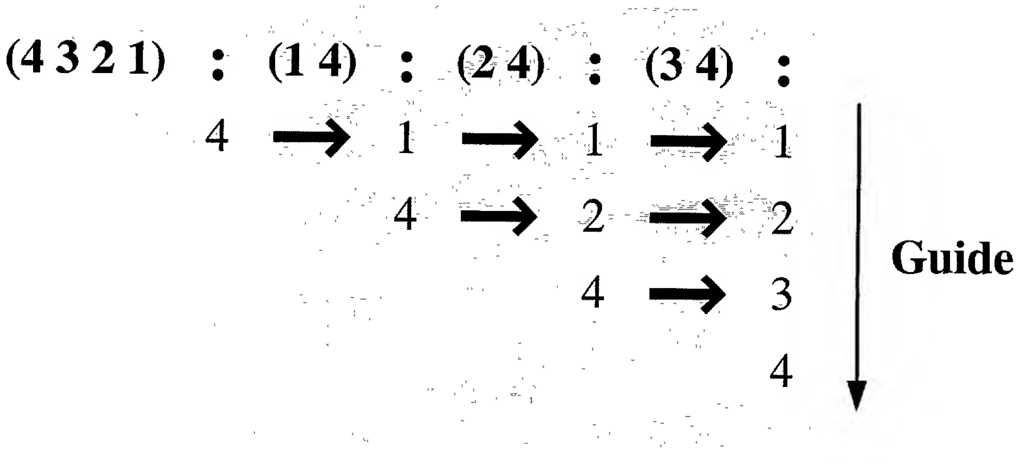


FIG. 28B

FIG. 29

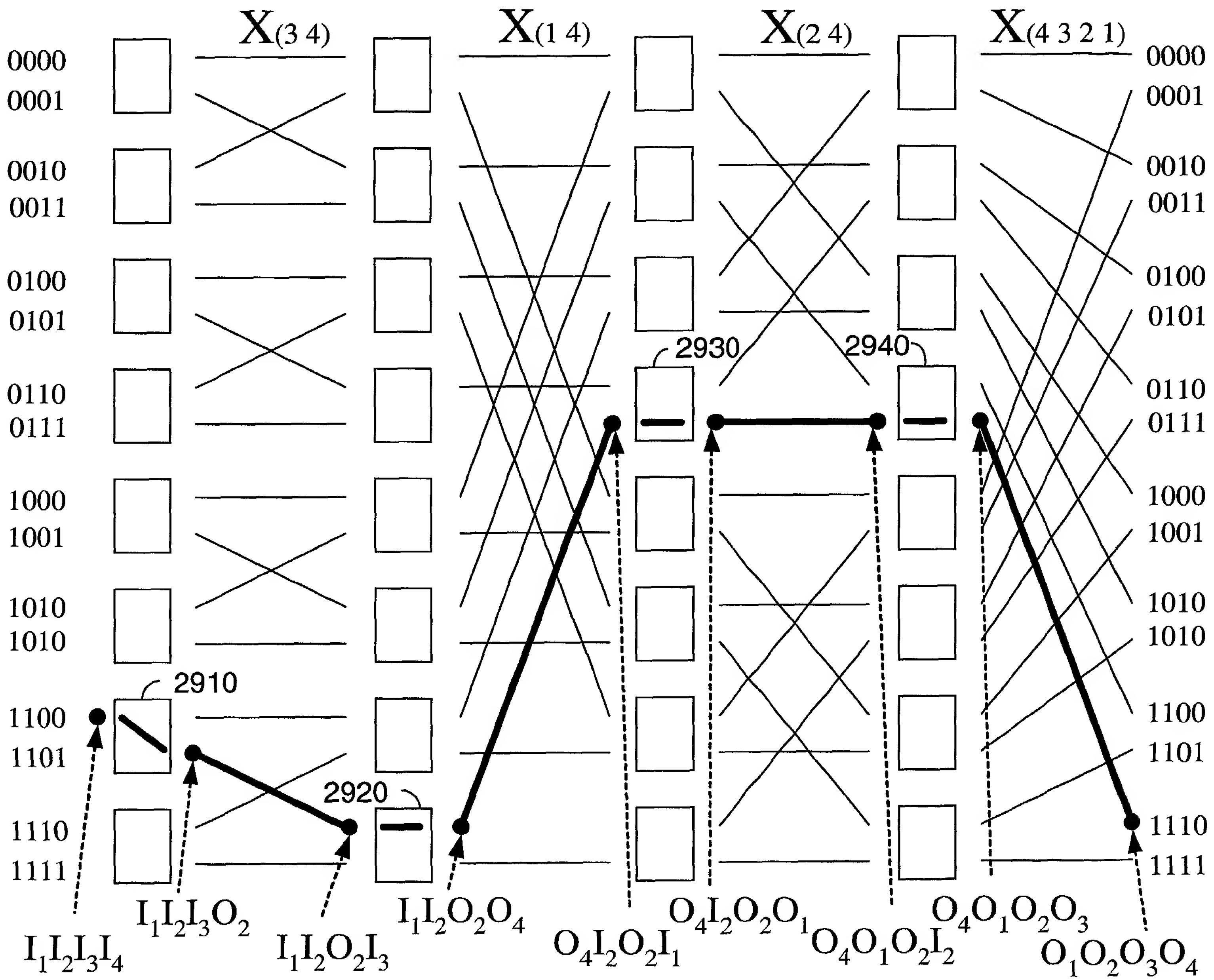

2900
X(3 4)
X(1 4)
X(2 4)
X(4 3 2 1)
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1010
1100
1101
1110
1111
2910
2920
2930
2940
$I_1I_2I_3I_4$
$I_1I_2I_3O_2$
$I_1I_2O_2I_3$
$I_1I_2O_2O_4$
$O_4I_2O_2I_1$
$O_4I_2O_2O_1$
$O_4O_1O_2I_2$
$O_4O_1O_2O_3$
$O_1O_2O_3O_4$

FIG. 30A

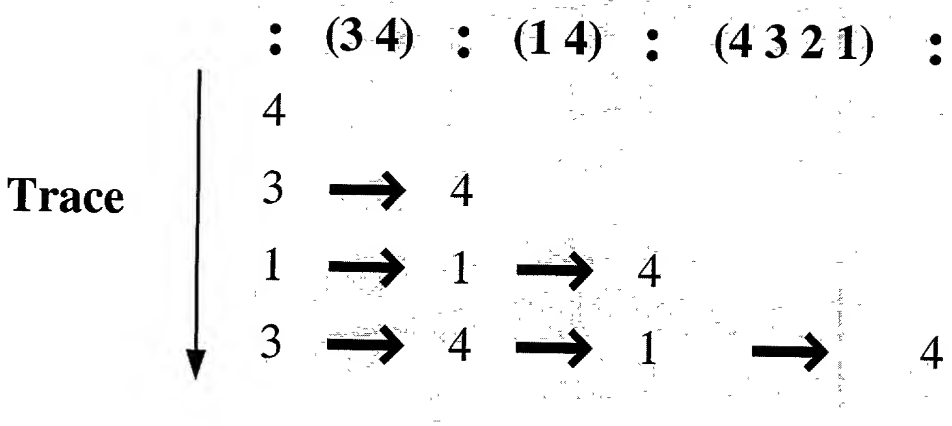
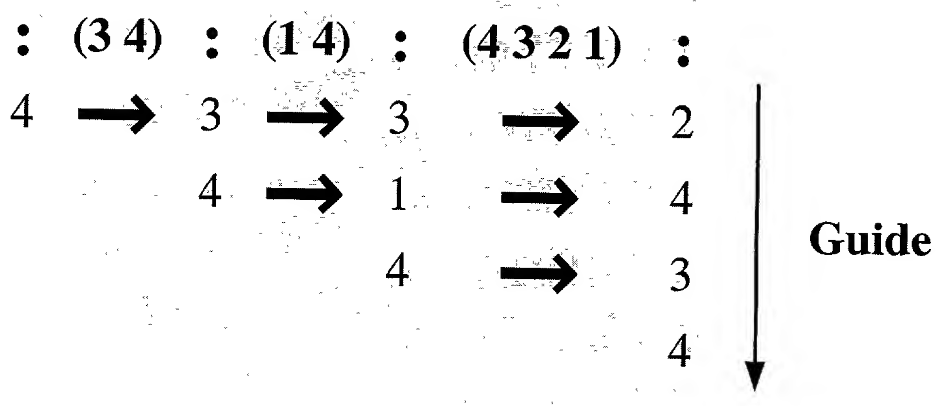


FIG. 30B



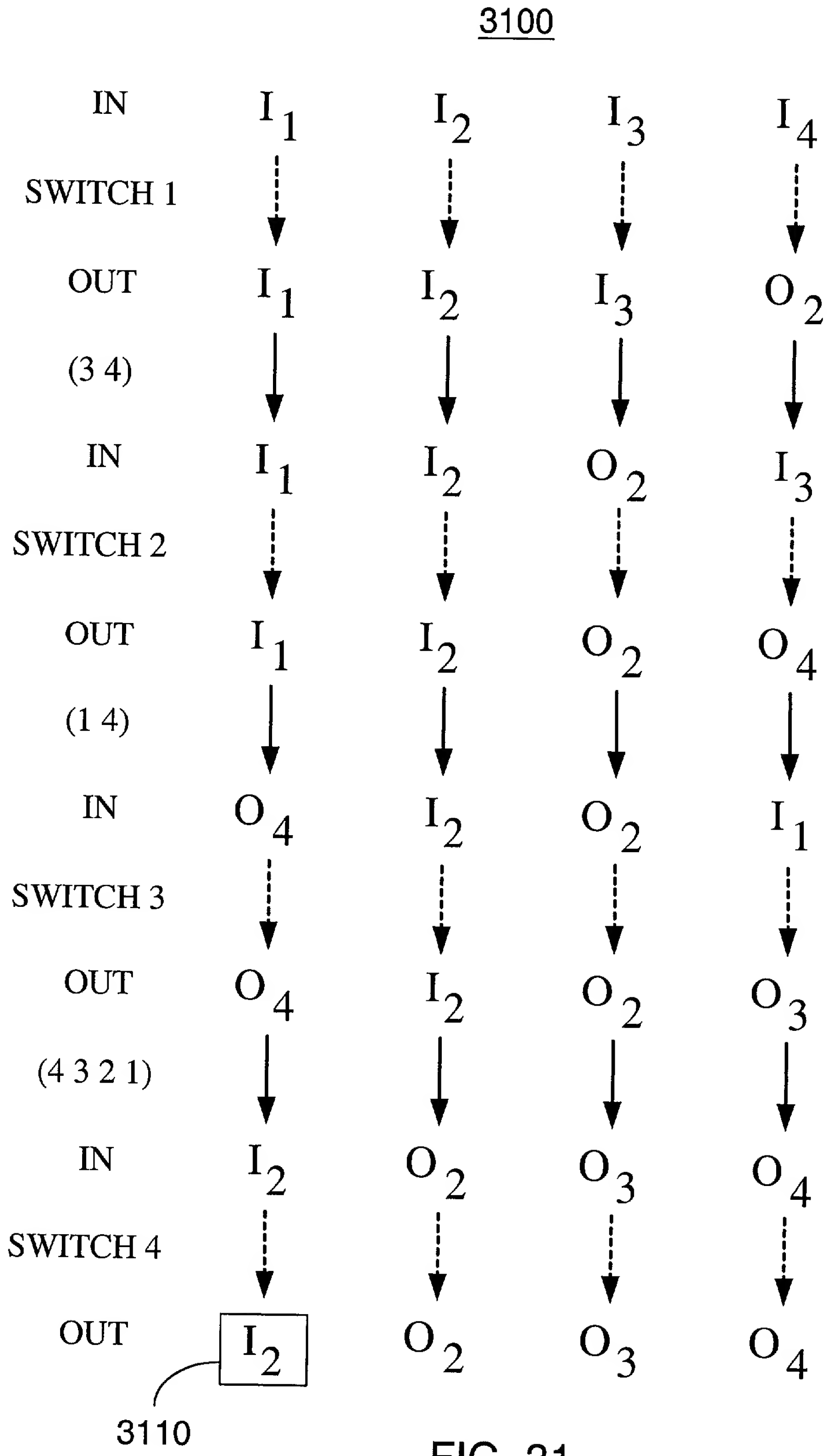

3100
IN
I_1 I_2 I_3 I_4
SWITCH 1
OUT
I_1 I_2 I_3 O_2
(3 4)
IN
I_1 I_2 O_2 I_3
SWITCH 2
OUT
I_1 I_2 O_2 O_4
(1 4)
IN
O_4 I_2 O_2 I_1
SWITCH 3
OUT
O_4 I_2 O_2 O_3
(4 3 2 1)
IN
I_2 O_2 O_3 O_4
SWITCH 4
OUT
I_2 O_2 O_3 O_4
3110

FIG. 31

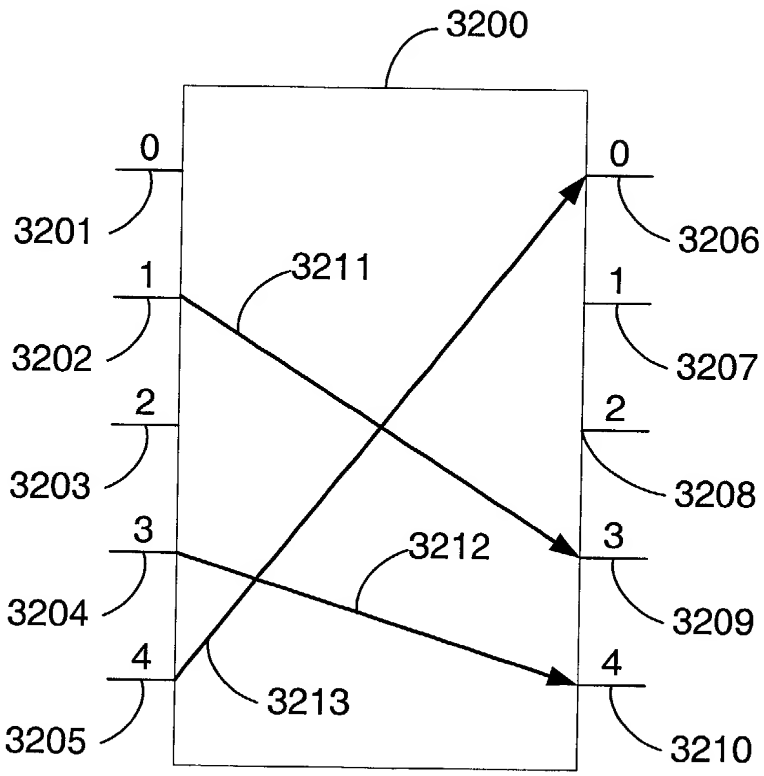


FIG. 32A

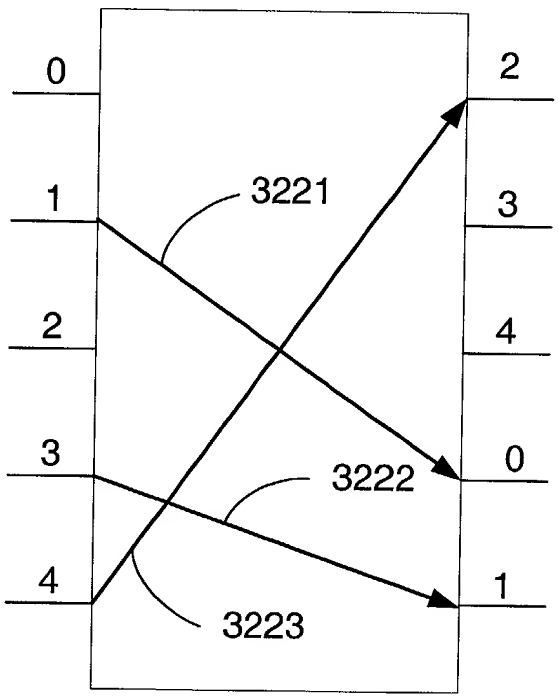


FIG. 32B

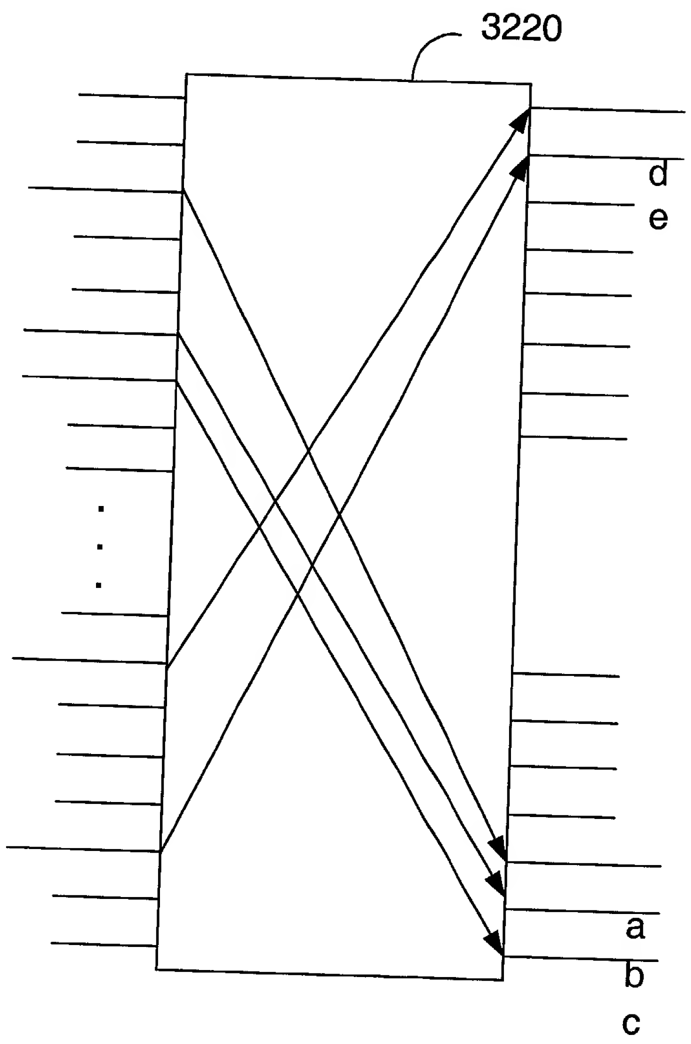


FIG. 32C

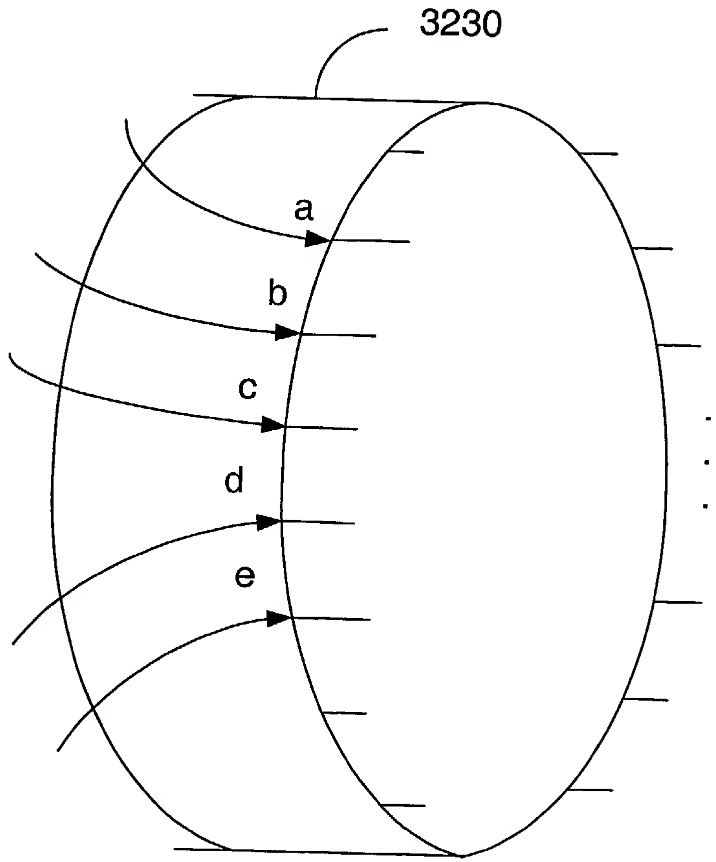


FIG. 32D

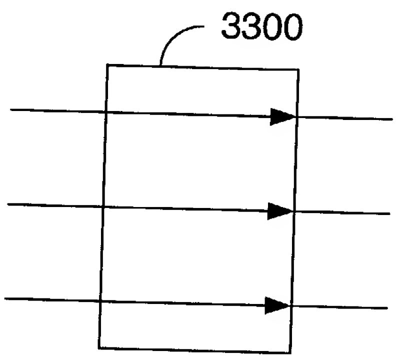


FIG. 33A

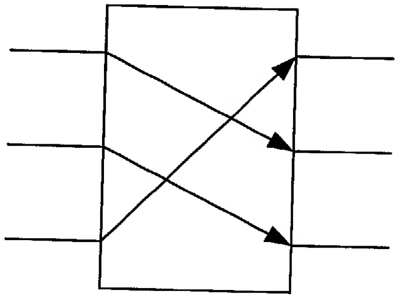


FIG. 33B

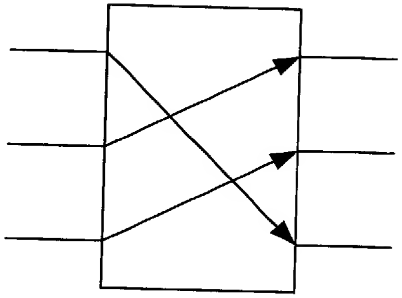


FIG. 33C

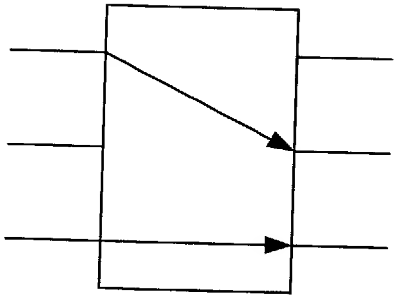


FIG. 33D

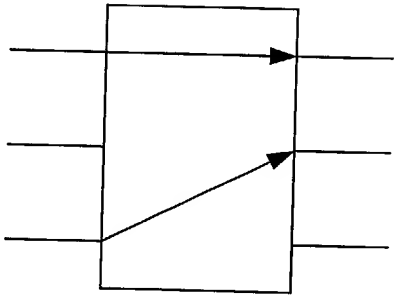


FIG. 33E

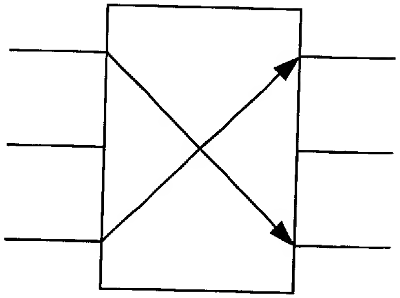


FIG.33F

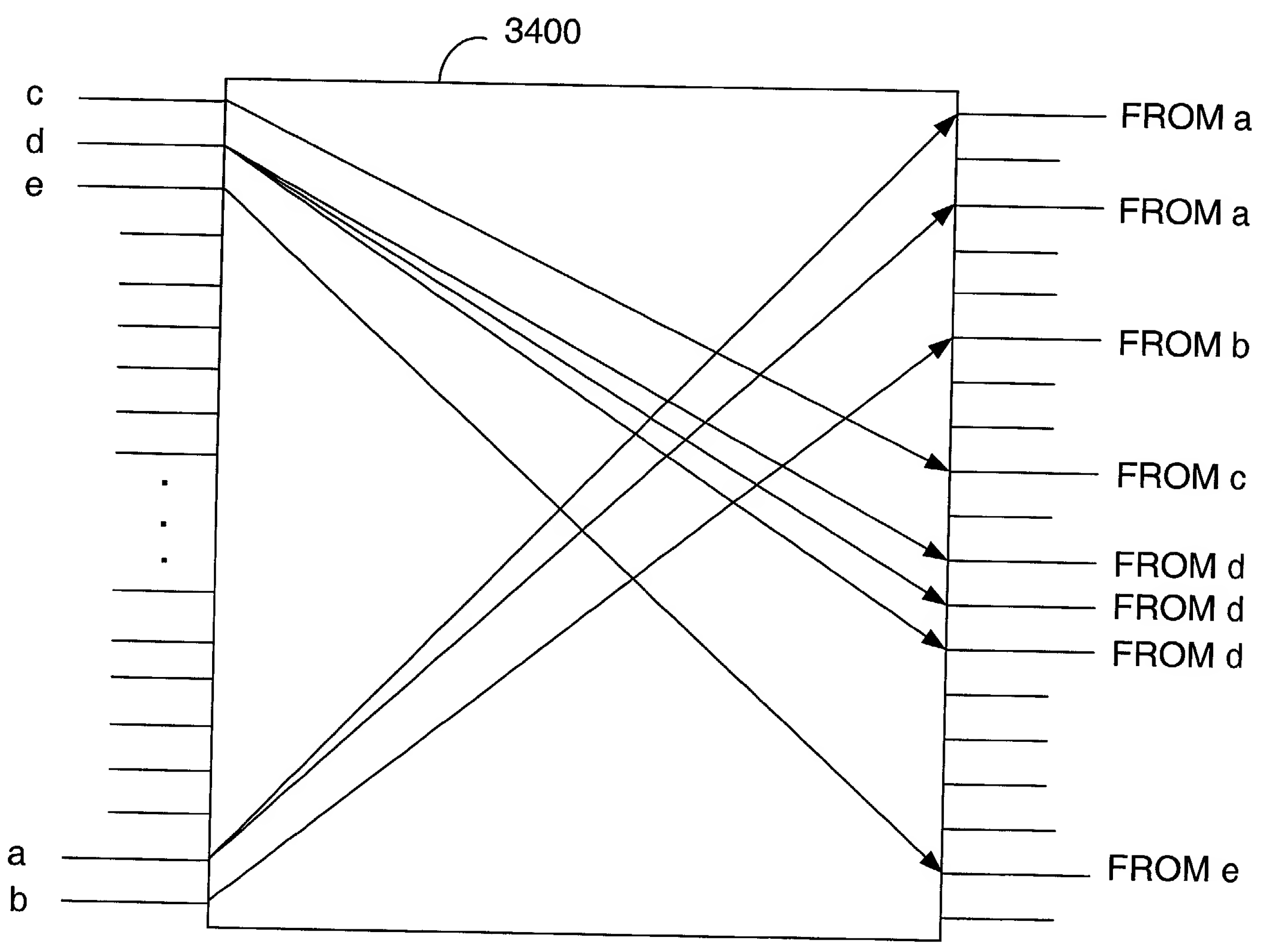


FIG. 34

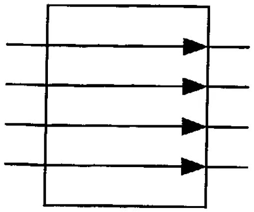


FIG. 35A

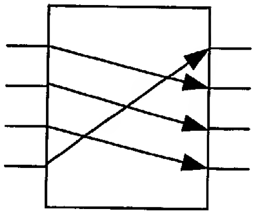


FIG. 35B

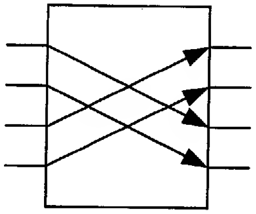


FIG. 35C

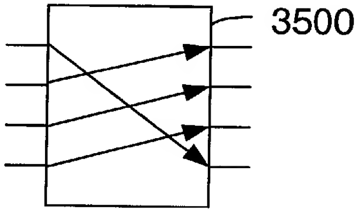


FIG. 35D

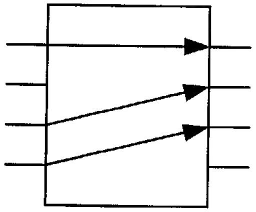


FIG. 35E

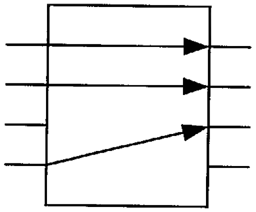


FIG. 35F

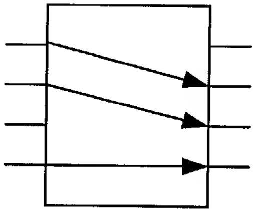


FIG. 35G

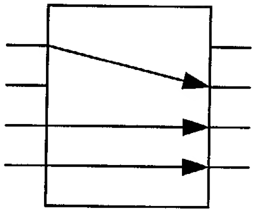


FIG. 35H

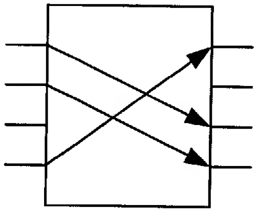


FIG. 35I

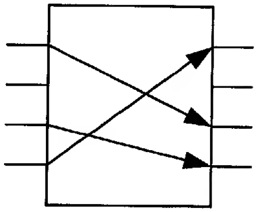


FIG. 35J

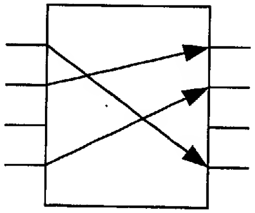


FIG. 35K

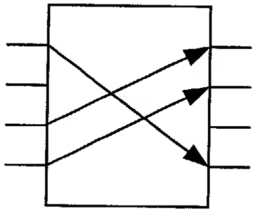


FIG. 35L

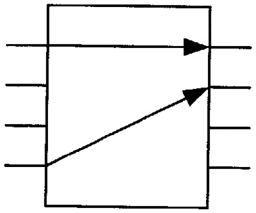


FIG. 35M

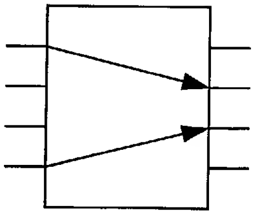


FIG. 35N

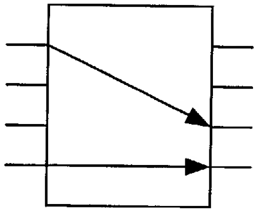


FIG. 35O

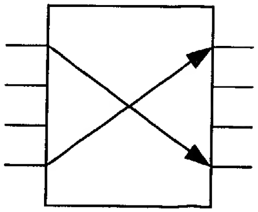


FIG. 35P

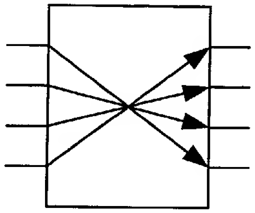


FIG. 36A

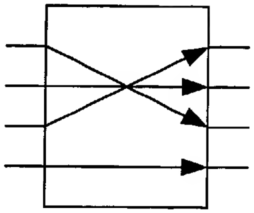


FIG. 36B

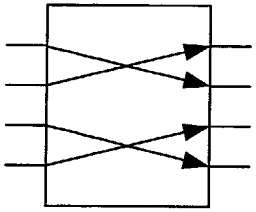


FIG. 36C

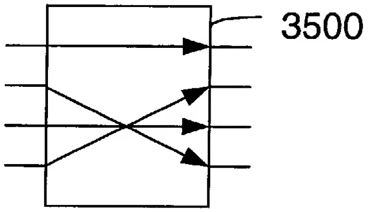


FIG. 36D

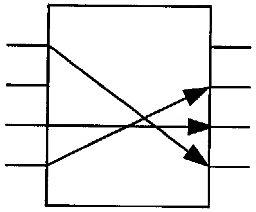


FIG. 36E

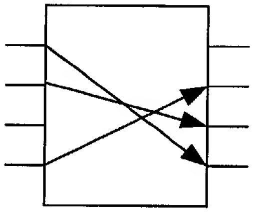


FIG. 36F

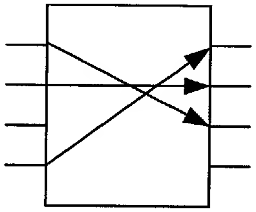


FIG. 36G

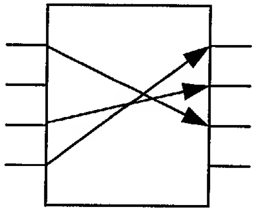


FIG. 36H

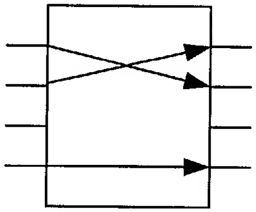


FIG. 36I

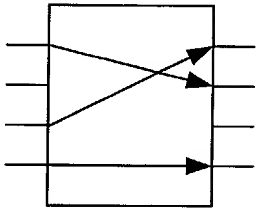


FIG. 36J

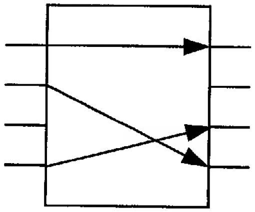


FIG. 36K

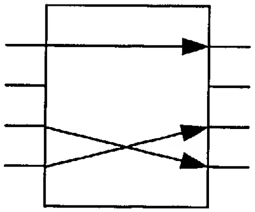


FIG. 36L

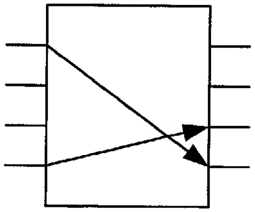


FIG. 36M

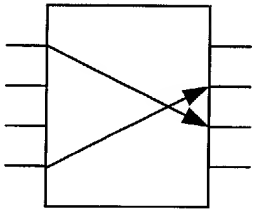


FIG. 36N

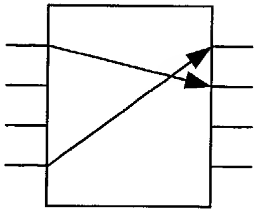


FIG. 36O

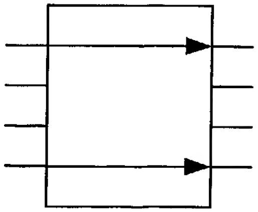


FIG. 36P

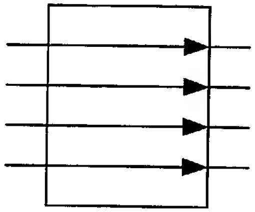


FIG. 37A

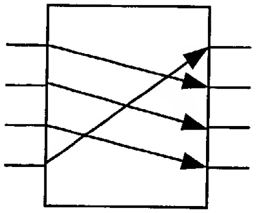


FIG. 37B

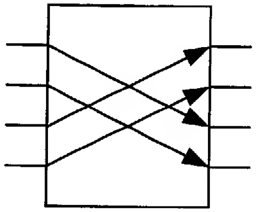


FIG. 37C

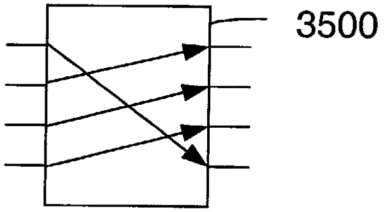


FIG. 37D

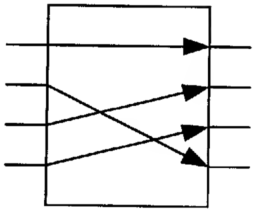


FIG. 37E

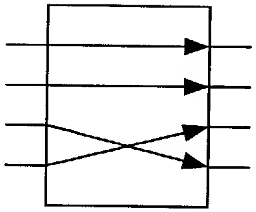


FIG. 37F

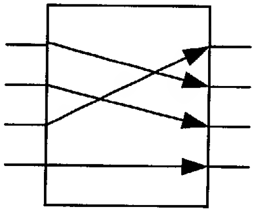


FIG. 37G

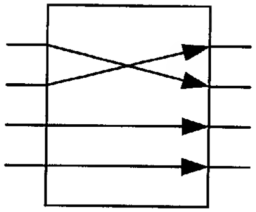


FIG. 37H

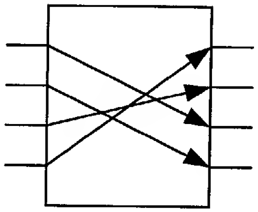


FIG. 37I

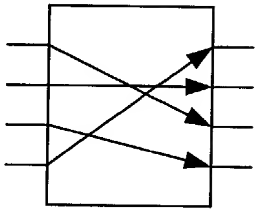


FIG. 37J

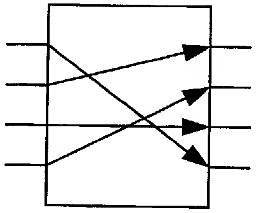


FIG. 37K

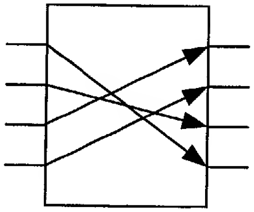


FIG. 37L

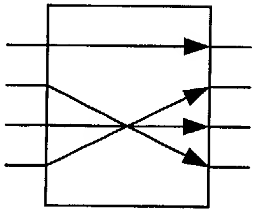


FIG. 37M

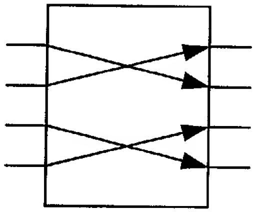


FIG. 37N

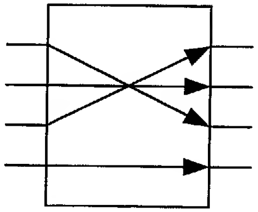


FIG. 37O

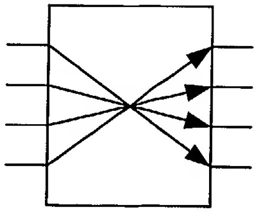


FIG. 37P

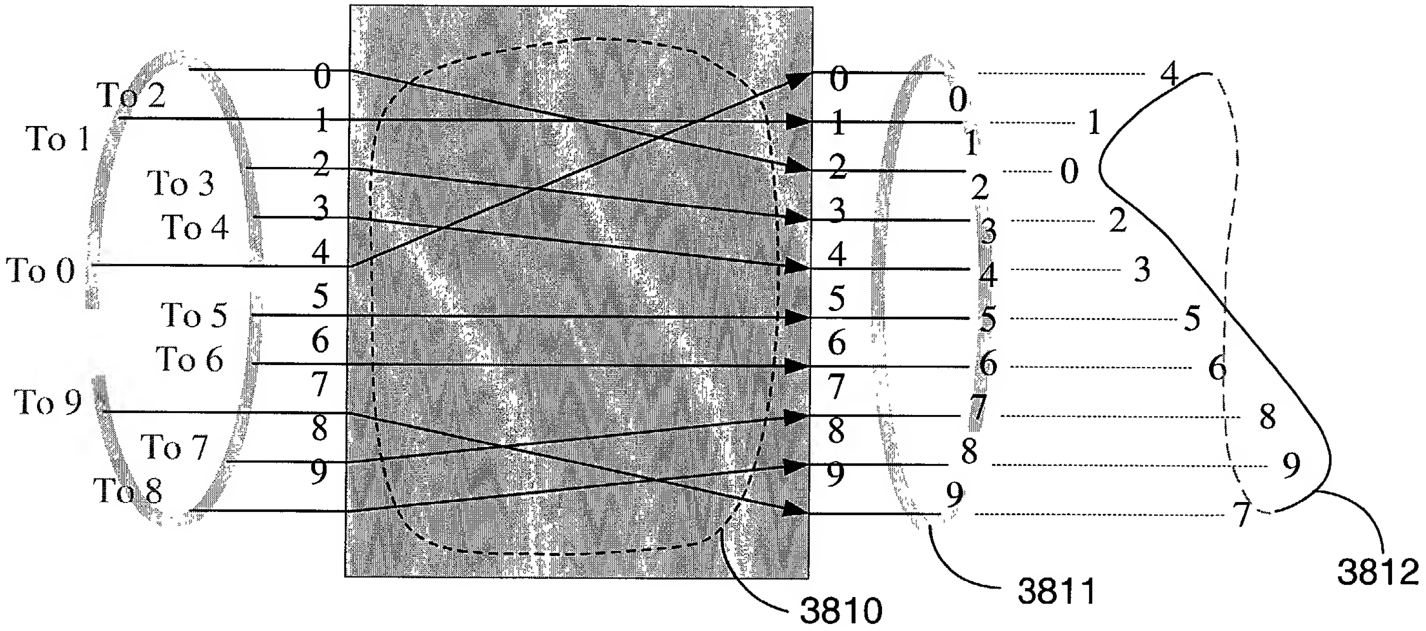

To 2
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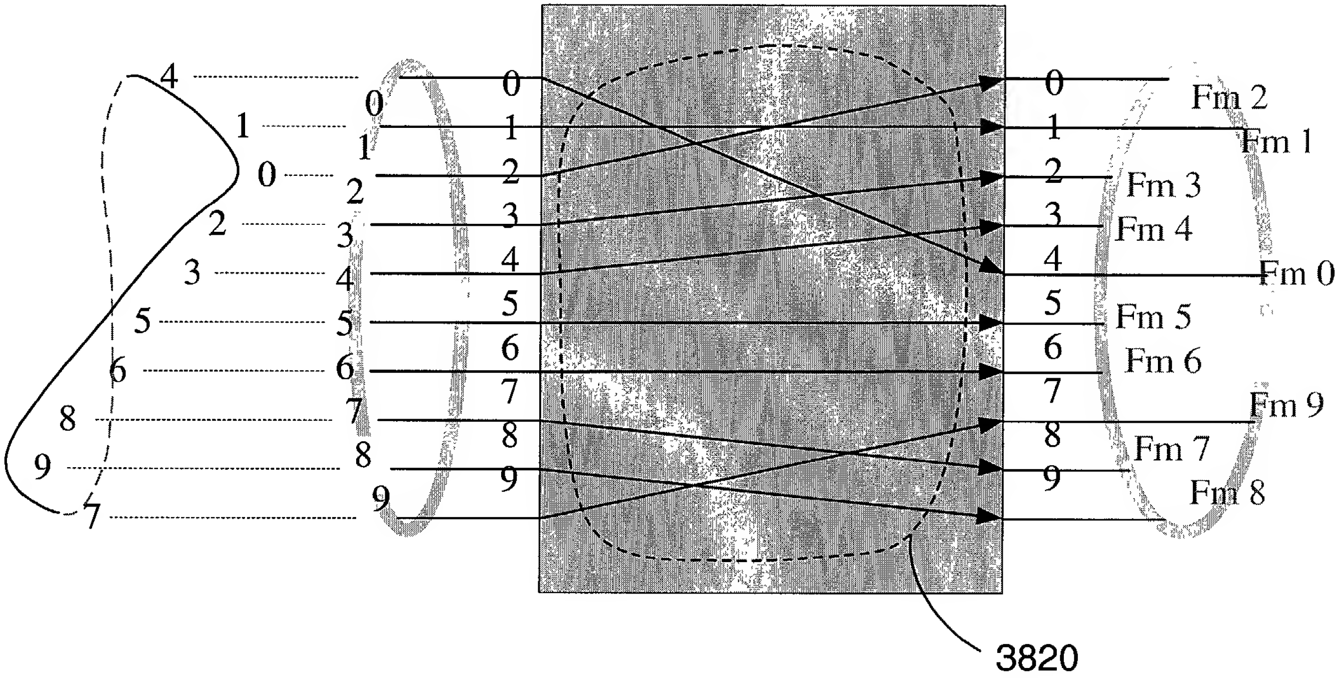
FIG. 38A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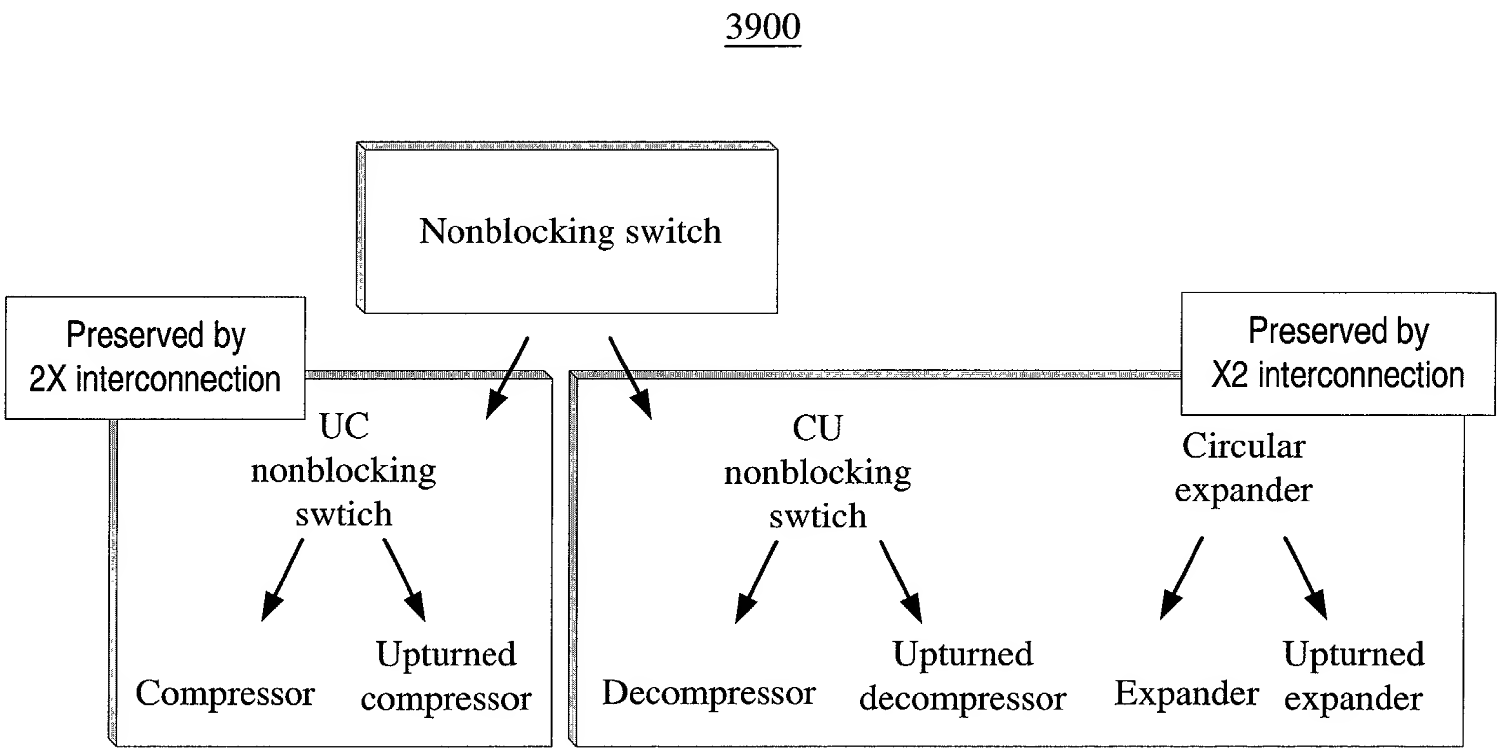
Fm 9
Fm 7
Fm 8
3820

FIG.38B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Nonblocking switch
Preserved by
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swtich
Compressor
Upturned
compressor
CU
nonblocking
swtich
Decompressor
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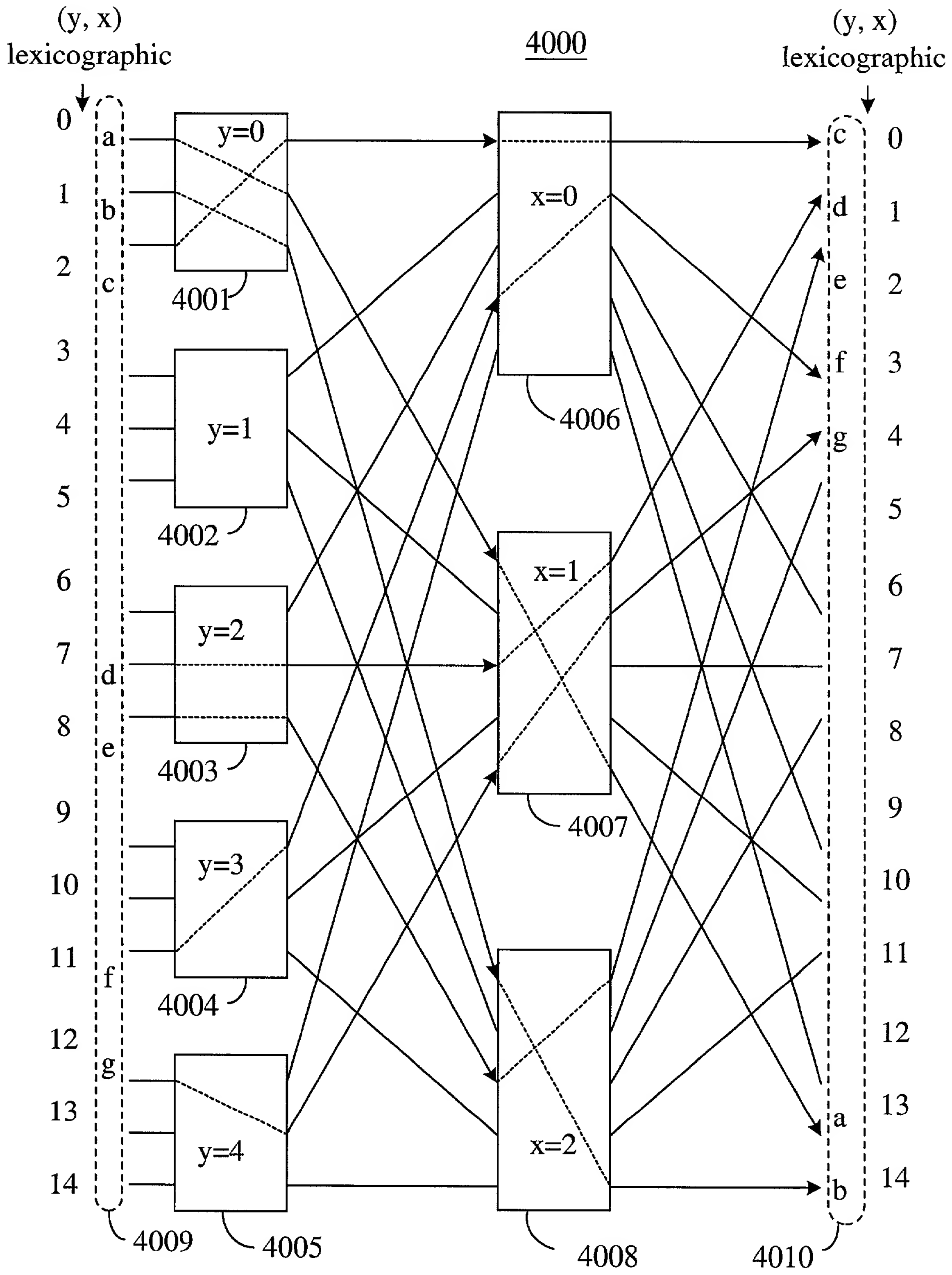
decompressor
Preserved by
X2 interconnection
Circular
expander
Expander
Upturned
expander

FIG. 39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x=0
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4007
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g
a
b
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
4010

FIG. 40

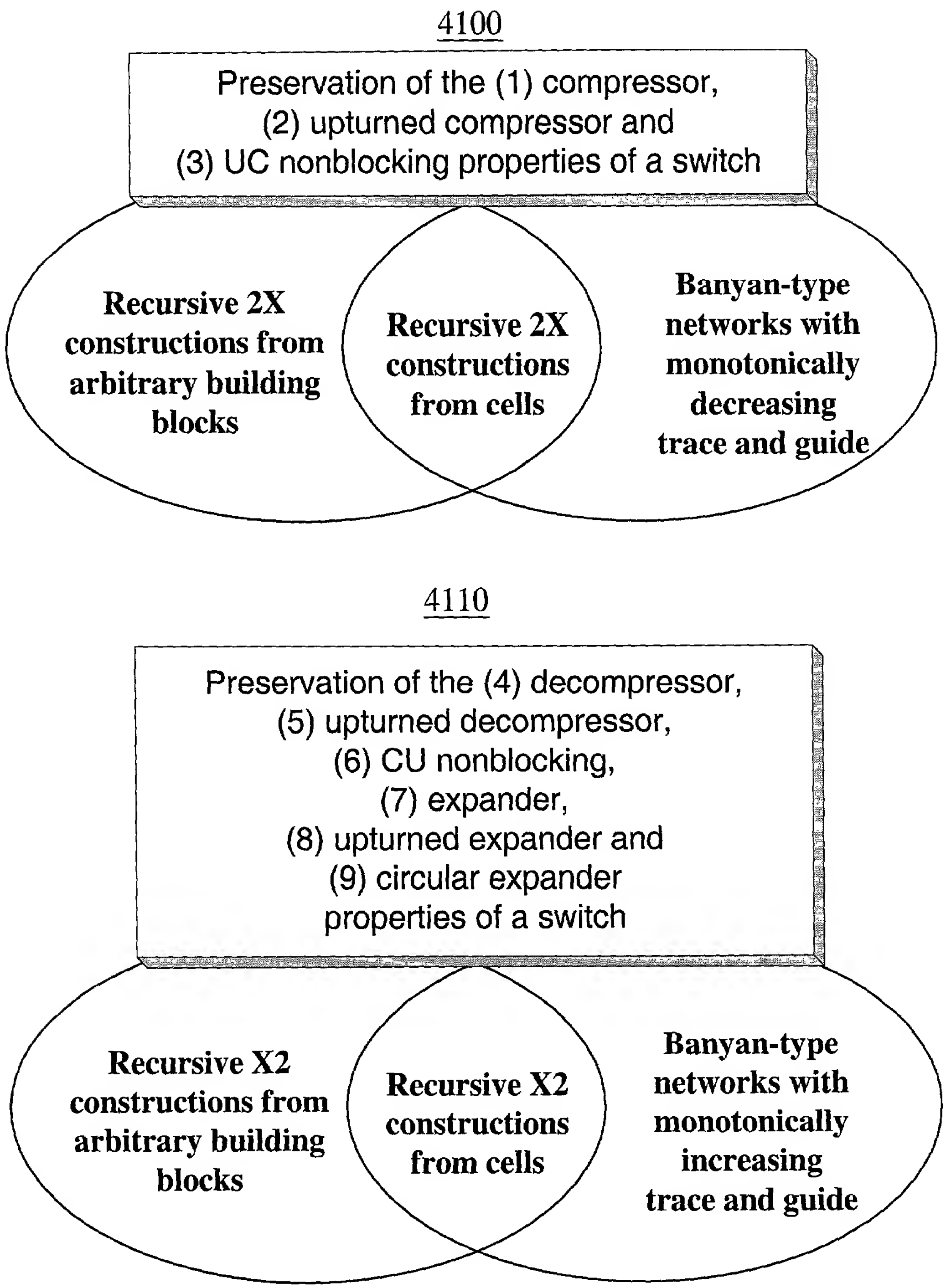

4100
Preservation of the (1) compressor, (2) upturned compressor and (3) UC nonblocking properties of a switch
Recursive 2X constructions from arbitrary building blocks
Recursive 2X constructions from cells
Banyan-type networks with monotonically decreasing trace and guide
4110
Preservation of the (4) decompressor, (5) upturned decompressor, (6) CU nonblocking, (7) expander, (8) upturned expander and (9) circular expander properties of a switch
Recursive X2 constructions from arbitrary building blocks
Recursive X2 constructions from cells
Banyan-type networks with monotonically increasing trace and guide

FIG. 41

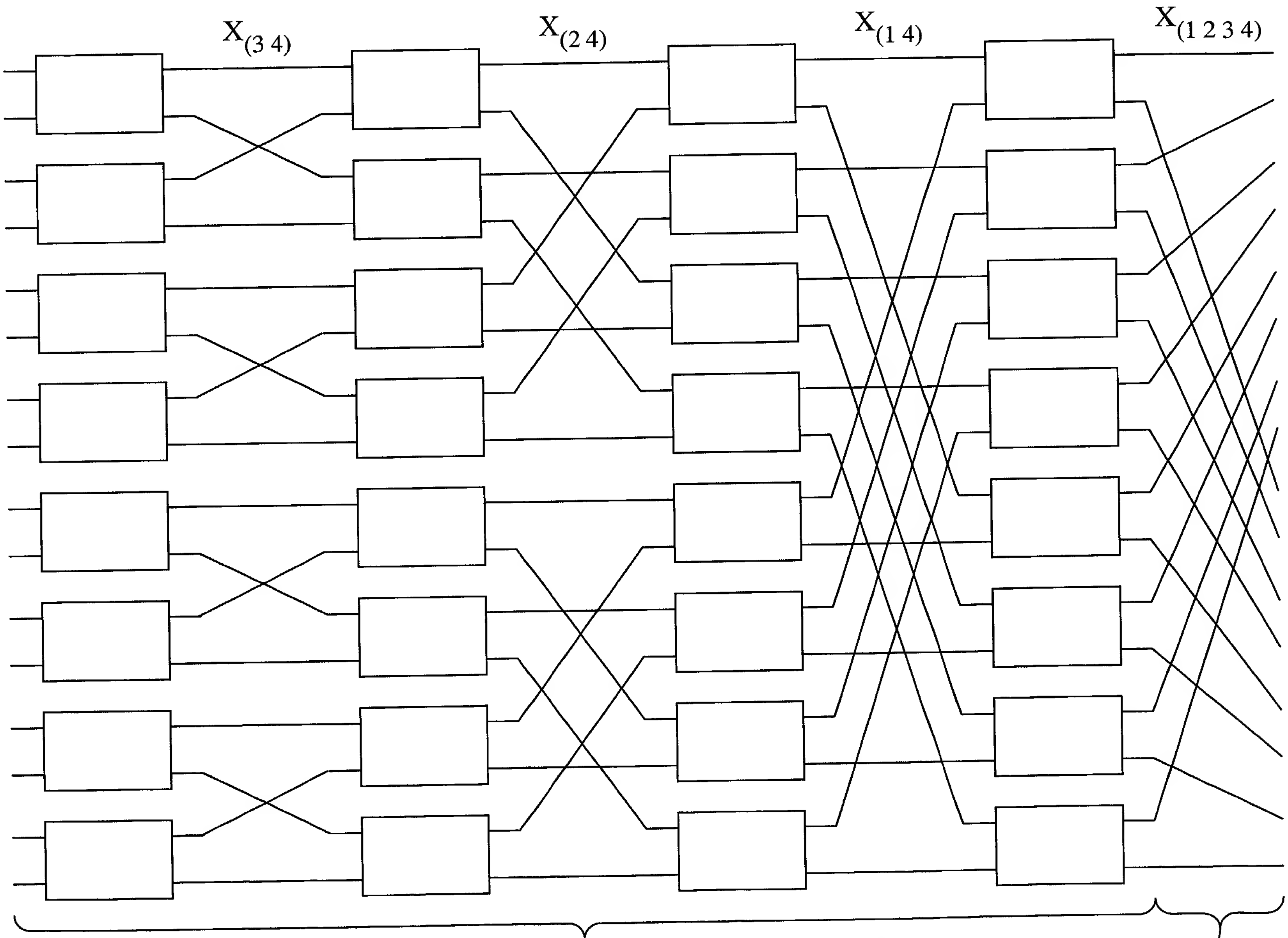


FIG. 42

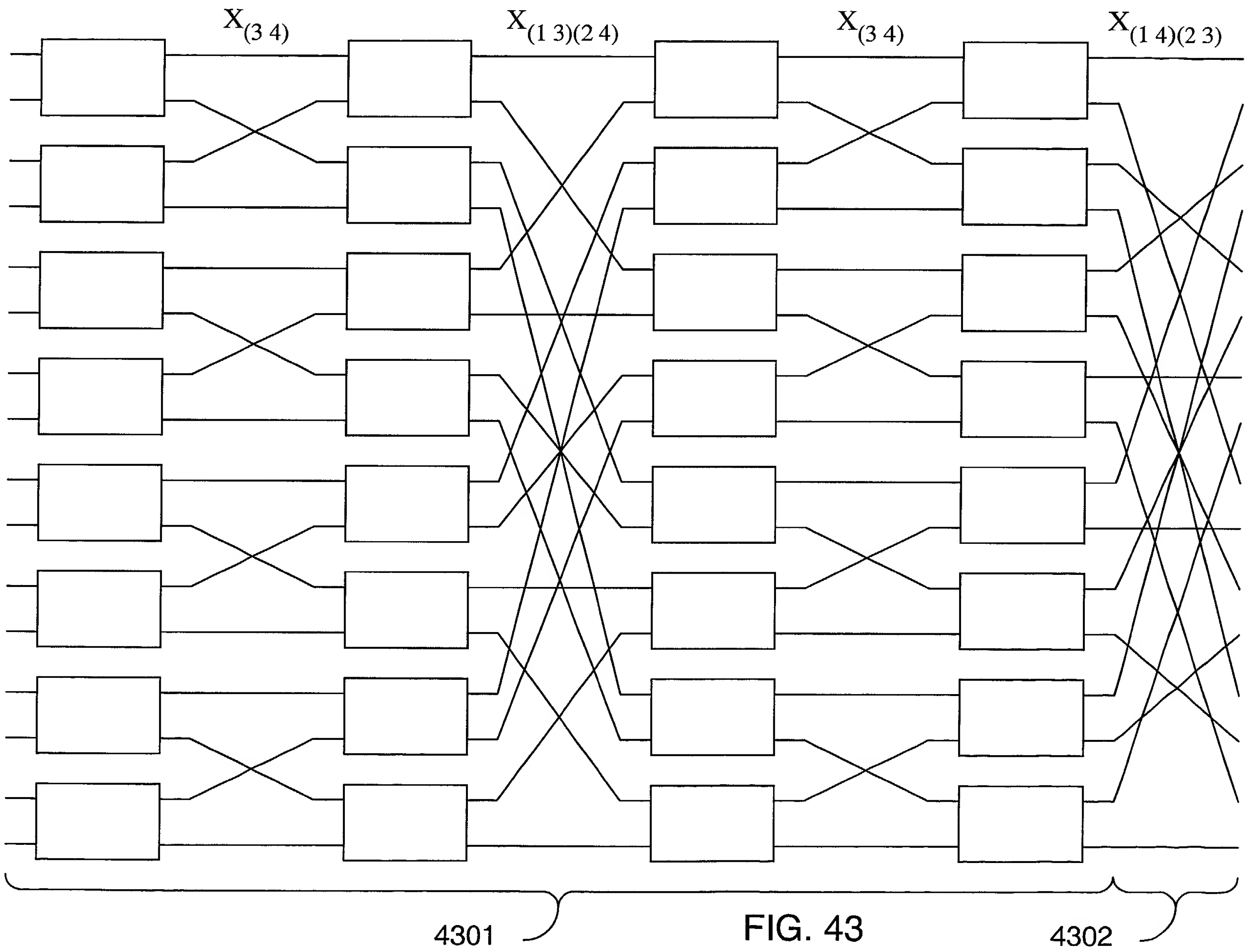


FIG. 43

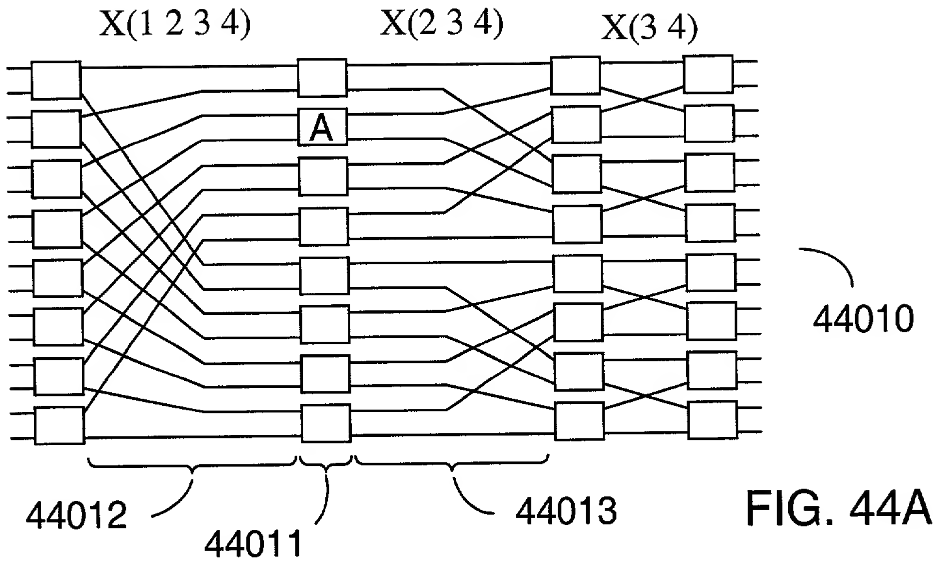


FIG. 44A

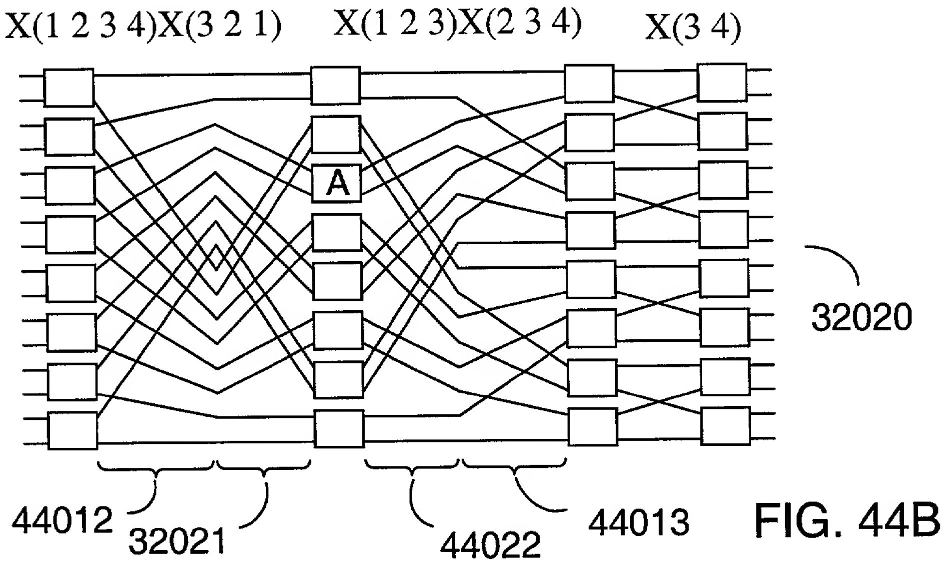


FIG. 44B

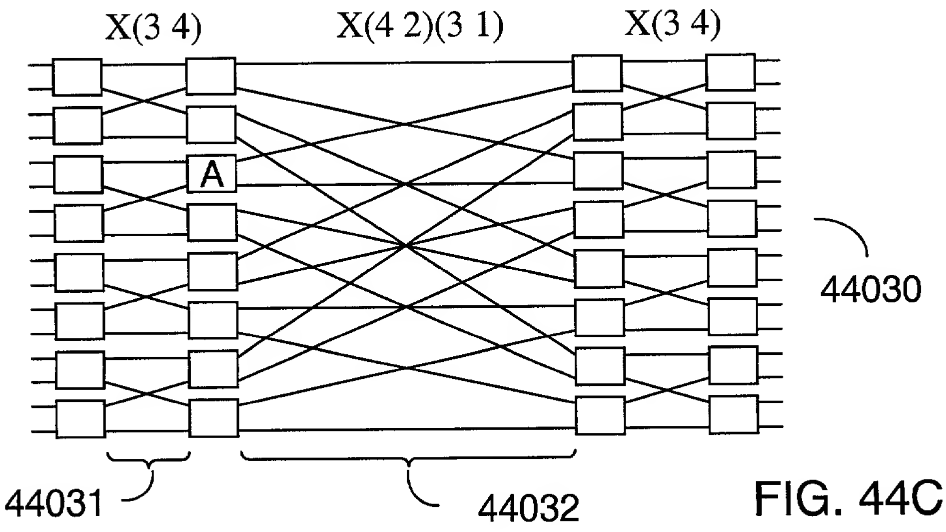


FIG. 44C

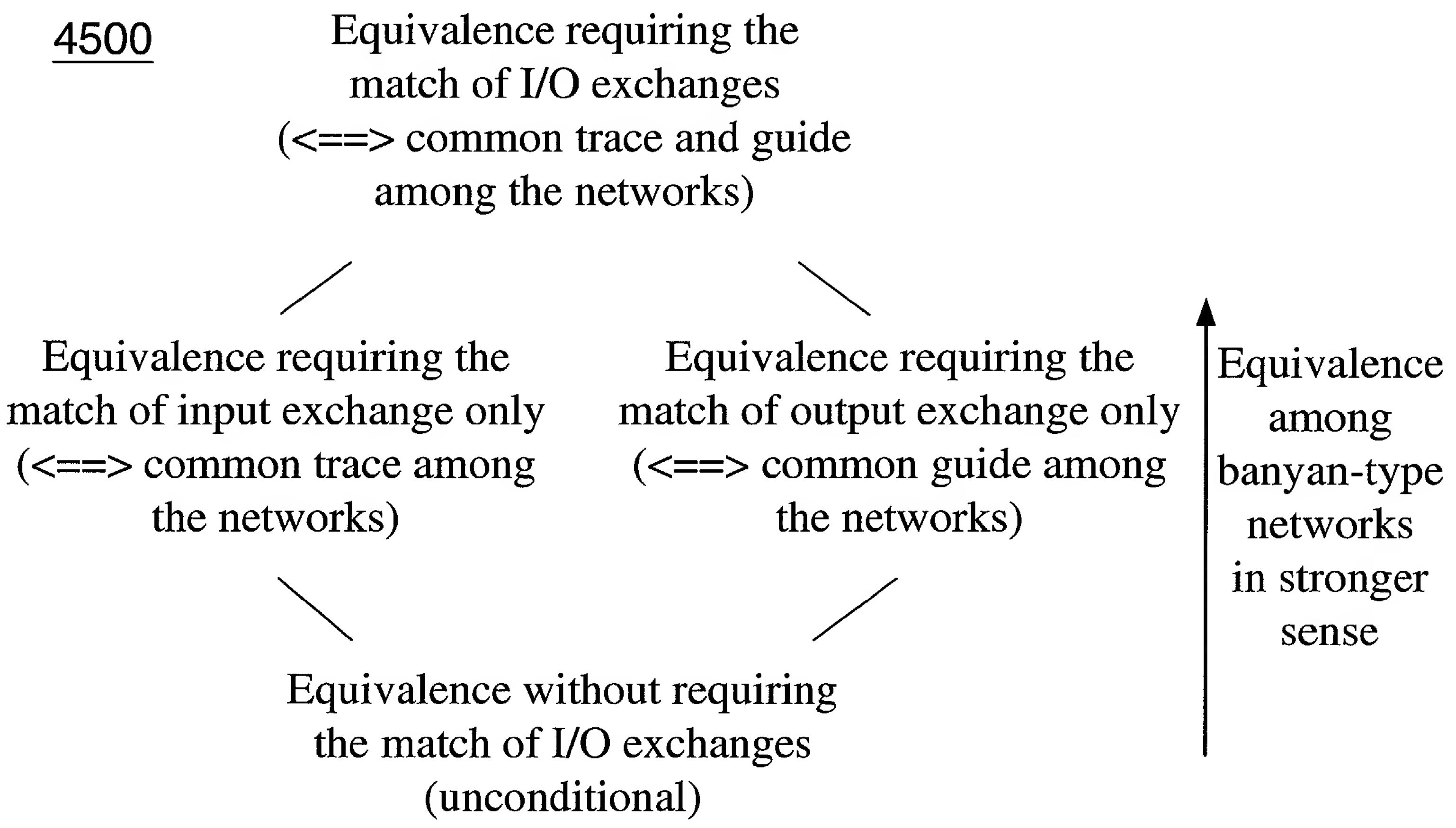

4500
Equivalence requiring the match of I/O exchanges (<==> common trace and guide among the networks)
Equivalence requiring the match of input exchange only (<==> common trace among the networks)
Equivalence requiring the match of output exchange only (<==> common guide among the networks)
Equivalence without requiring the match of I/O exchanges (unconditional)
Equivalence among banyan-type networks in stronger sense

FIG. 45

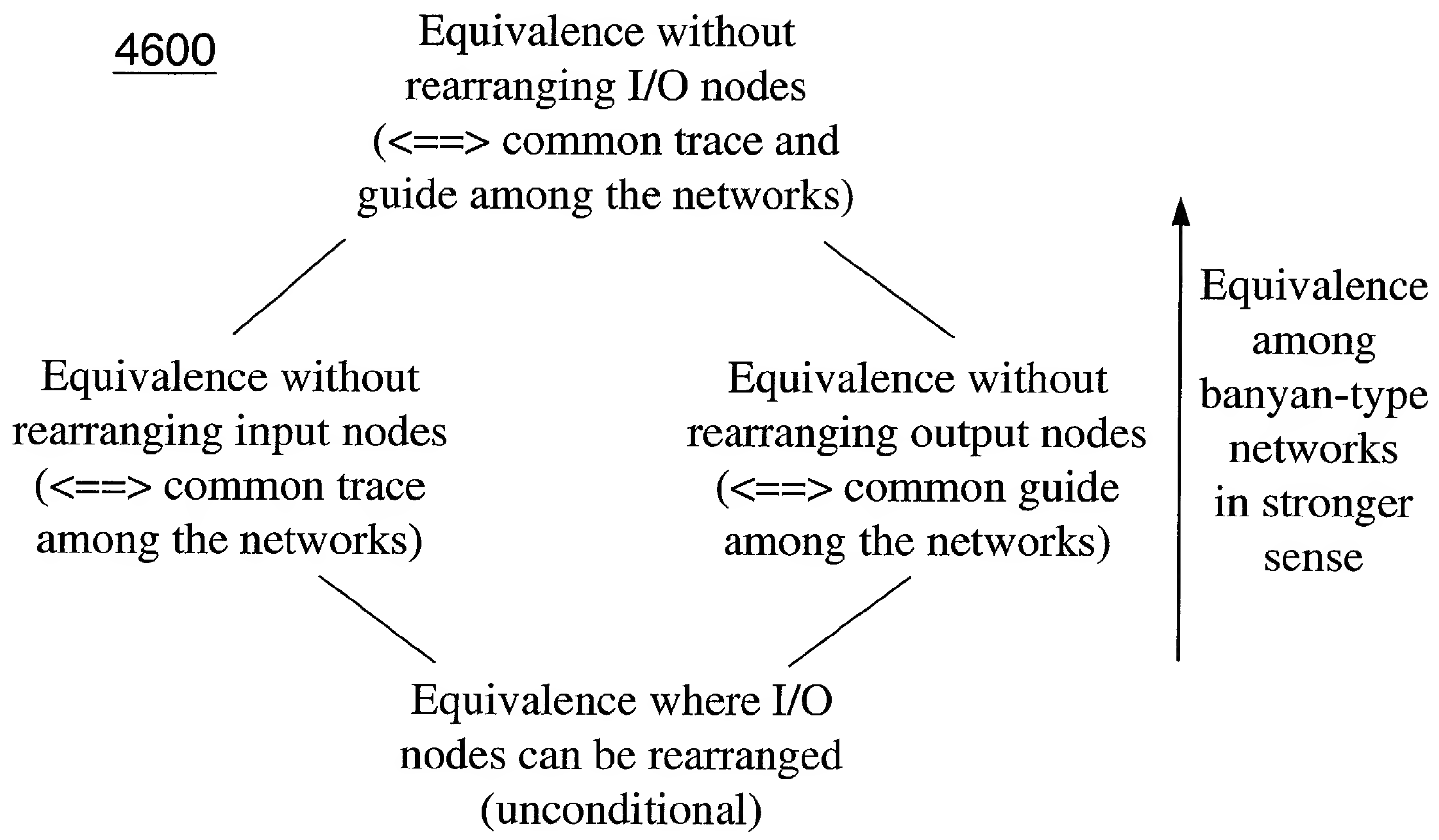

4600
Equivalence without rearranging I/O nodes (<==> common trace and guide among the networks)
Equivalence without rearranging input nodes (<==> common trace among the networks)
Equivalence without rearranging output nodes (<==> common guide among the networks)
Equivalence where I/O nodes can be rearranged (unconditional)
Equivalence among banyan-type networks in stronger sense

FIG. 46

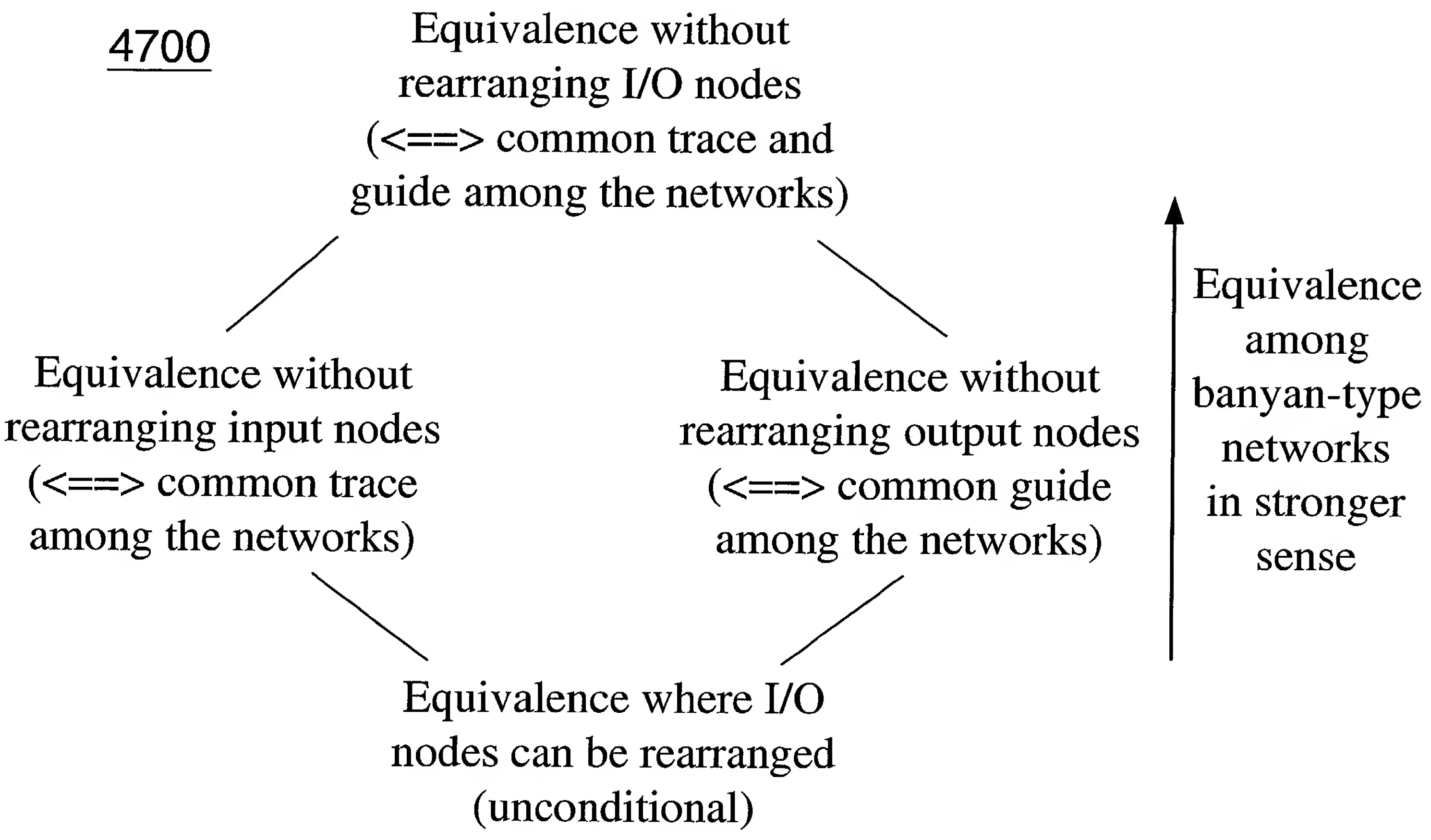

4700
Equivalence without rearranging I/O nodes (<==> common trace and guide among the networks)
Equivalence without rearranging input nodes (<==> common trace among the networks)
Equivalence without rearranging output nodes (<==> common guide among the networks)
Equivalence where I/O nodes can be rearranged (unconditional)
Equivalence among banyan-type networks in stronger sense

FIG. 47

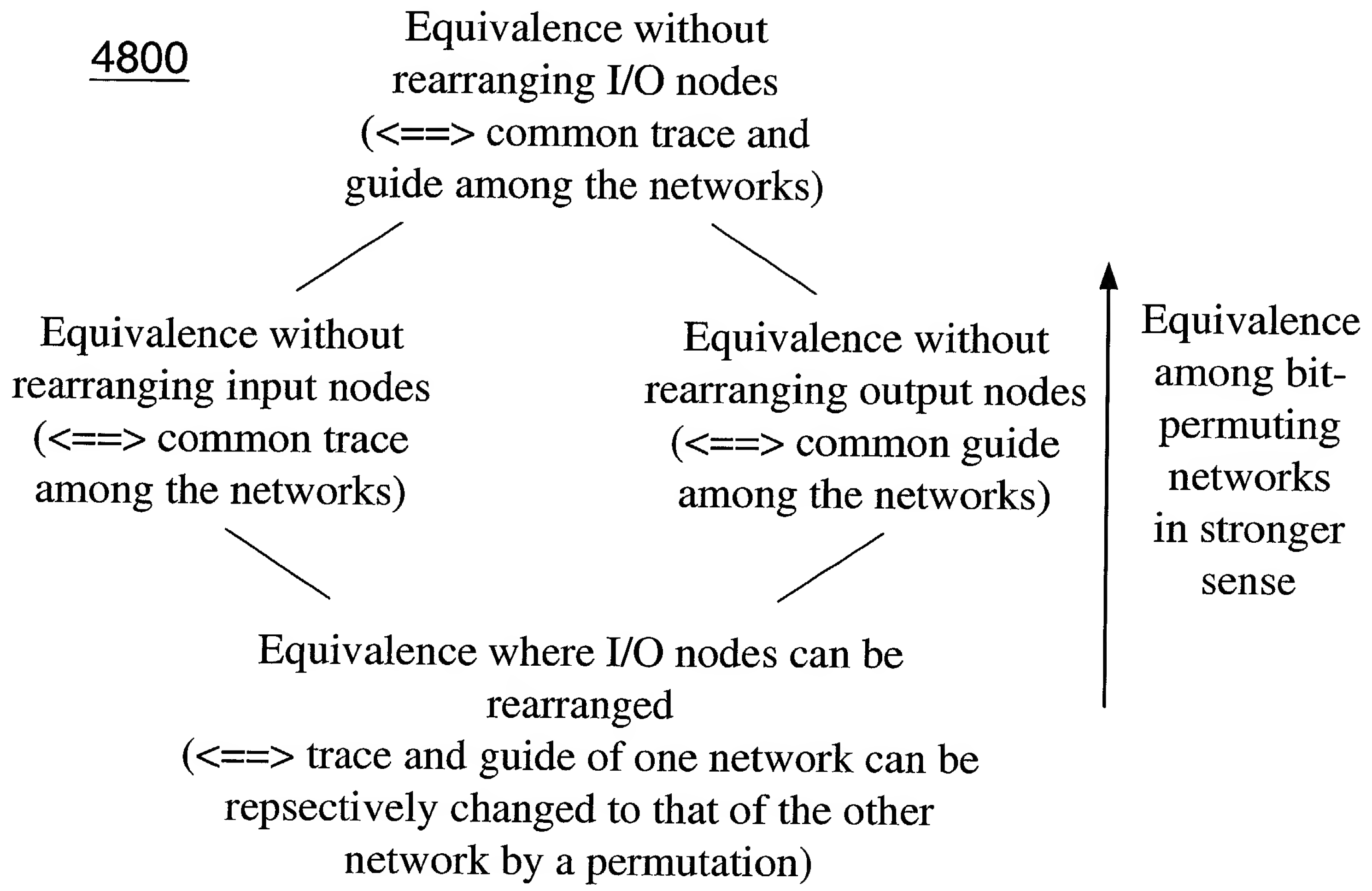

4800
Equivalence without rearranging I/O nodes (<==> common trace and guide among the networks)
Equivalence without rearranging input nodes (<==> common trace among the networks)
Equivalence without rearranging output nodes (<==> common guide among the networks)
Equivalence where I/O nodes can be rearranged (<==> trace and guide of one network can be repsectively changed to that of the other network by a permutation)
Equivalence among bit-permuting networks in stronger sense

FIG. 48

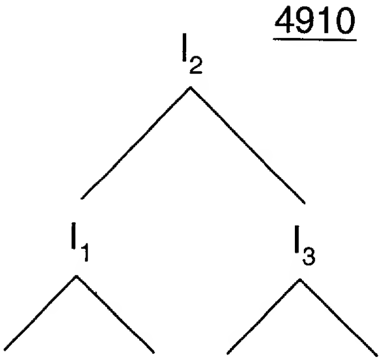


FIG. 49A

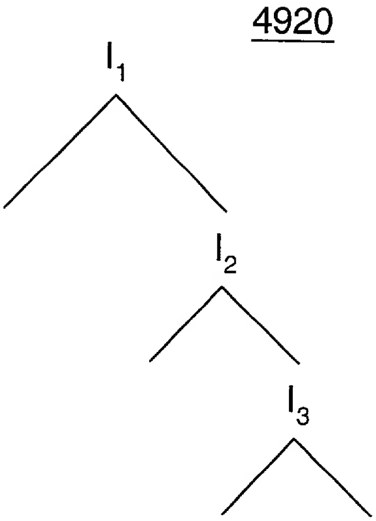


FIG. 49B

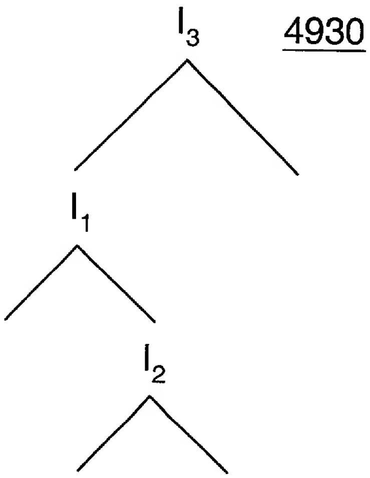


FIG. 49C

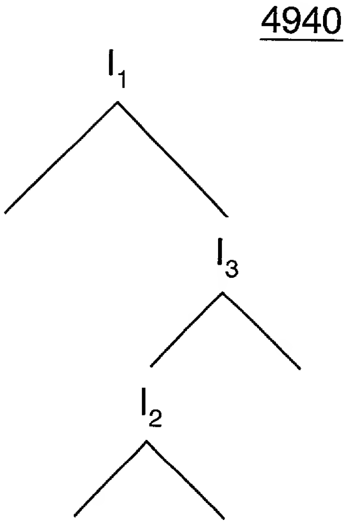


FIG. 49D

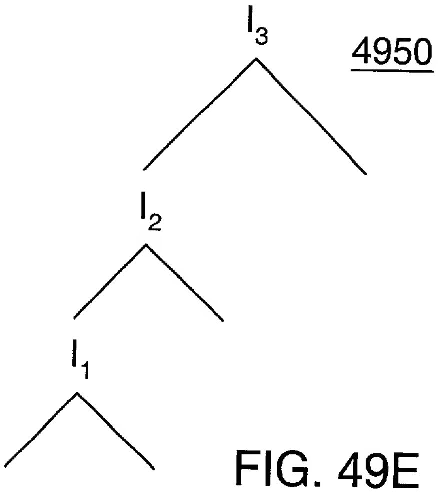


FIG. 49E

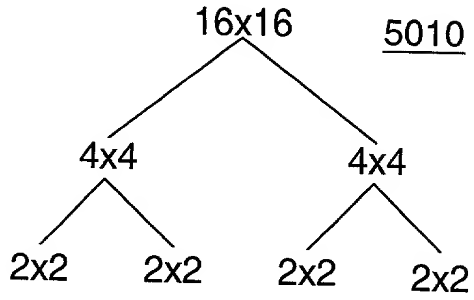


FIG. 50A

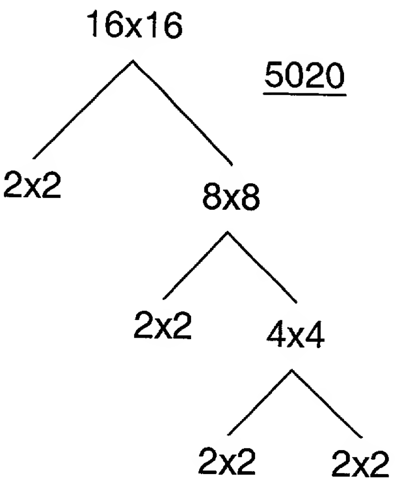


FIG. 50B

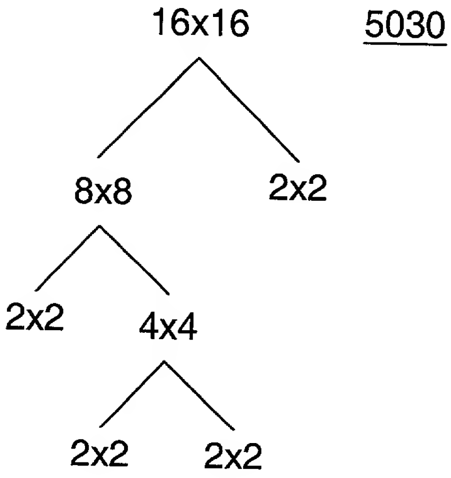


FIG. 50C

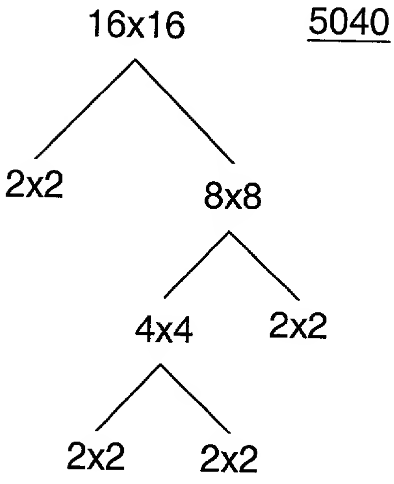


FIG. 50D

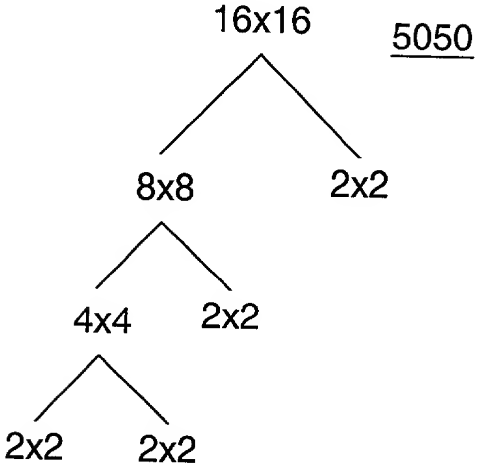


FIG. 50E

5100

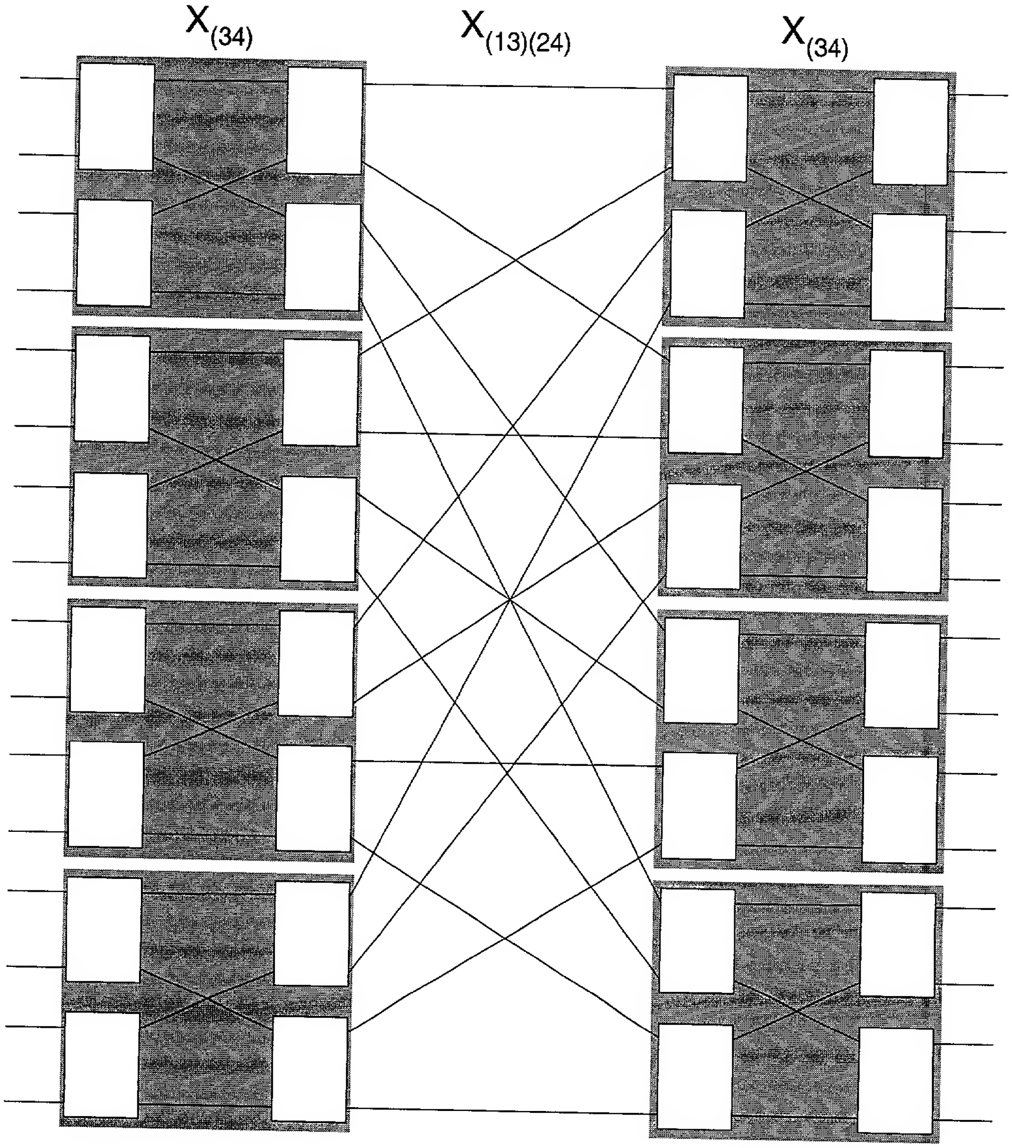


FIG. 51

5200

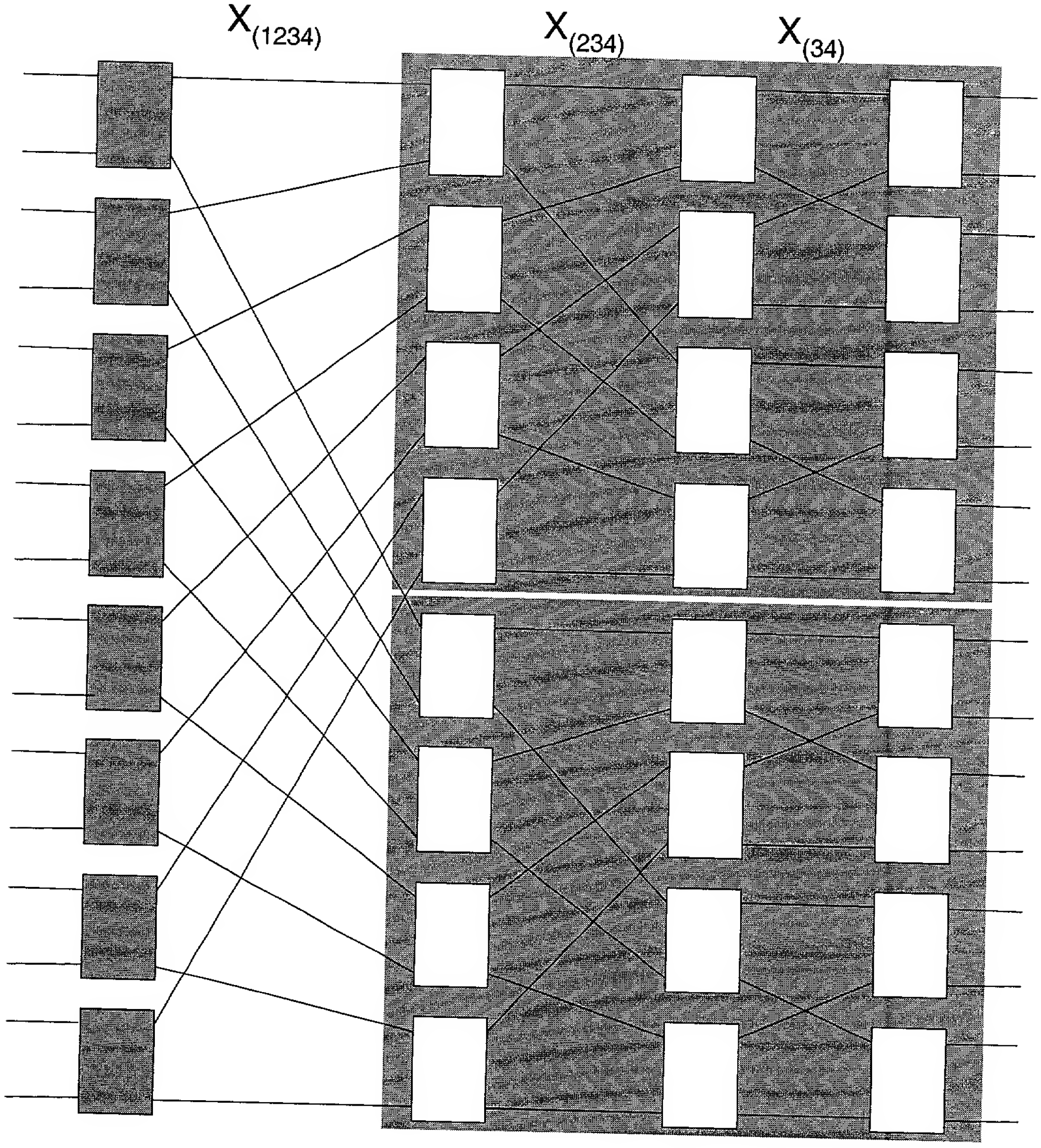
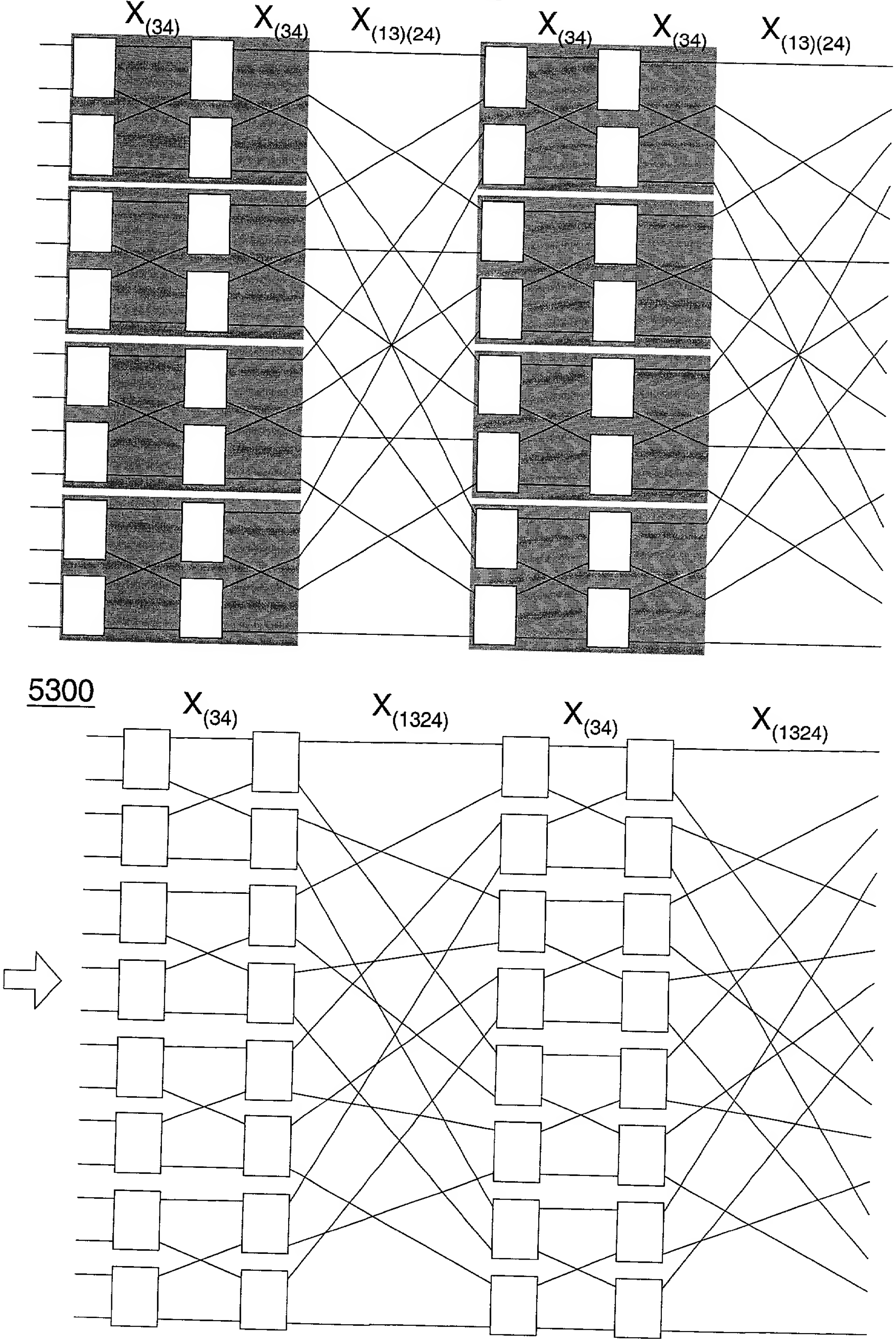


FIG. 52

FIG. 53



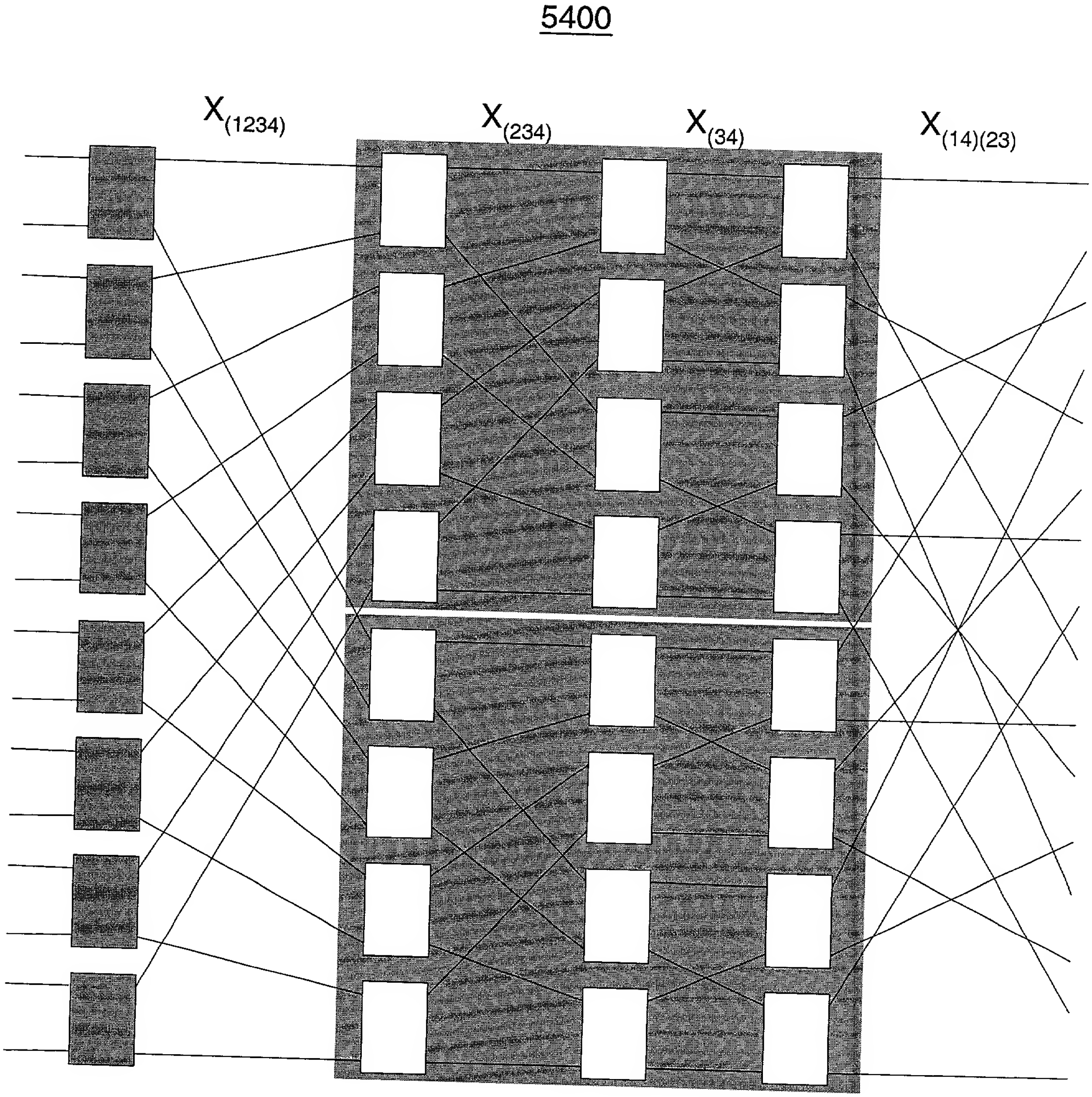


FIG. 54

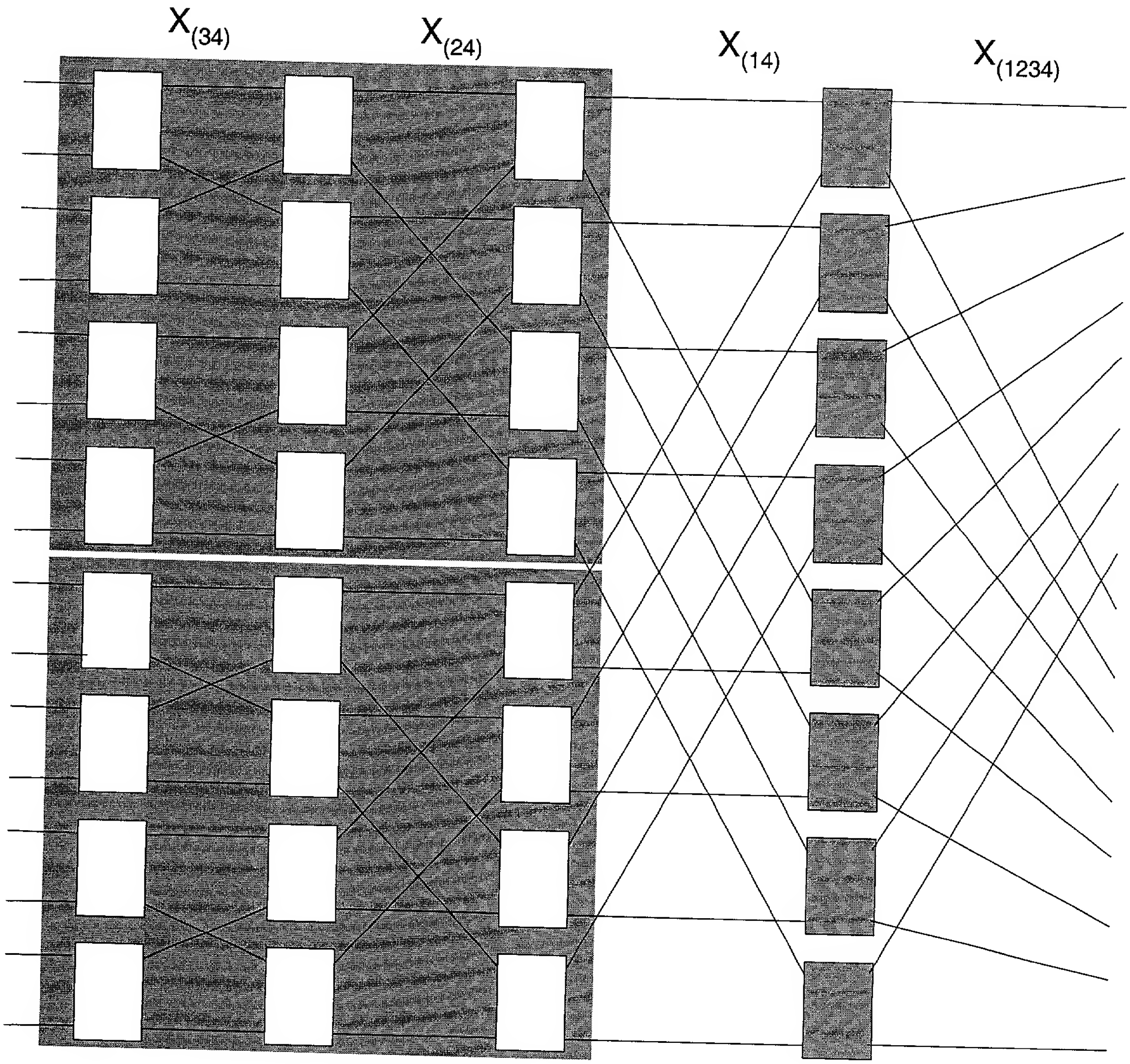


FIG. 55

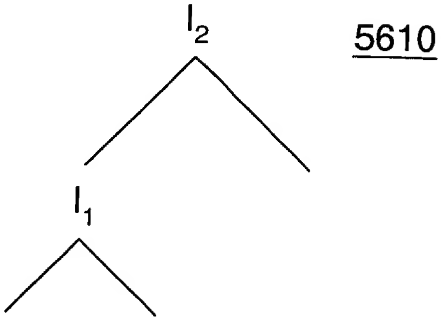


FIG. 56A

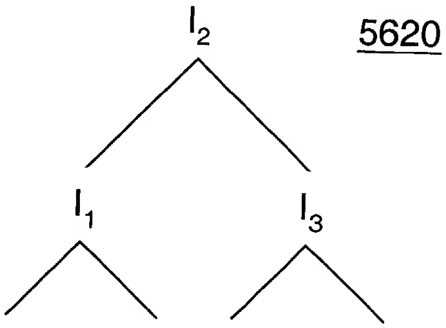


FIG. 56B

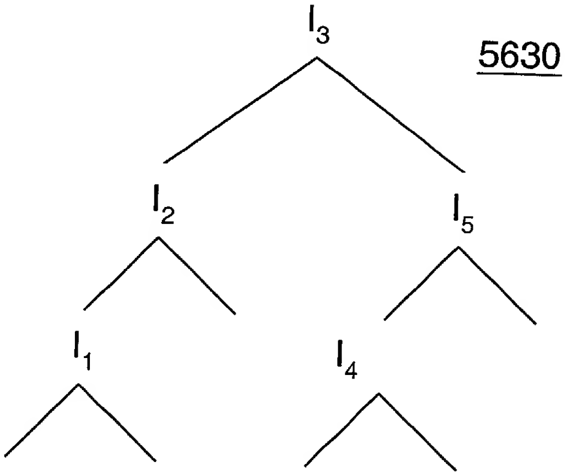


FIG. 56C

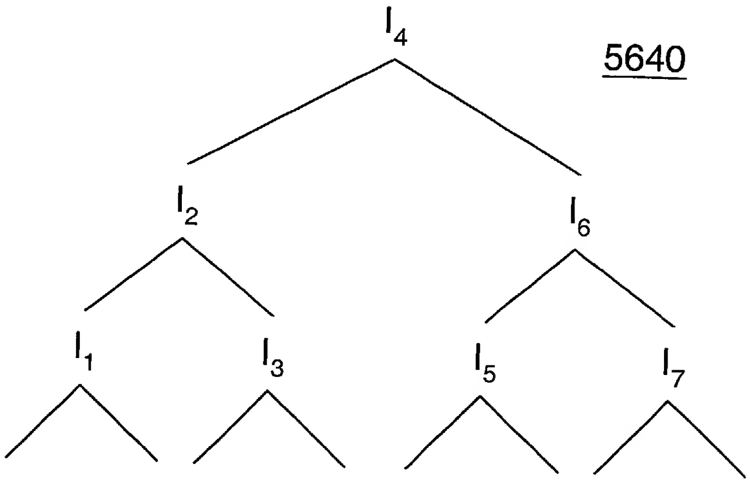


FIG. 56D

FIG. 57

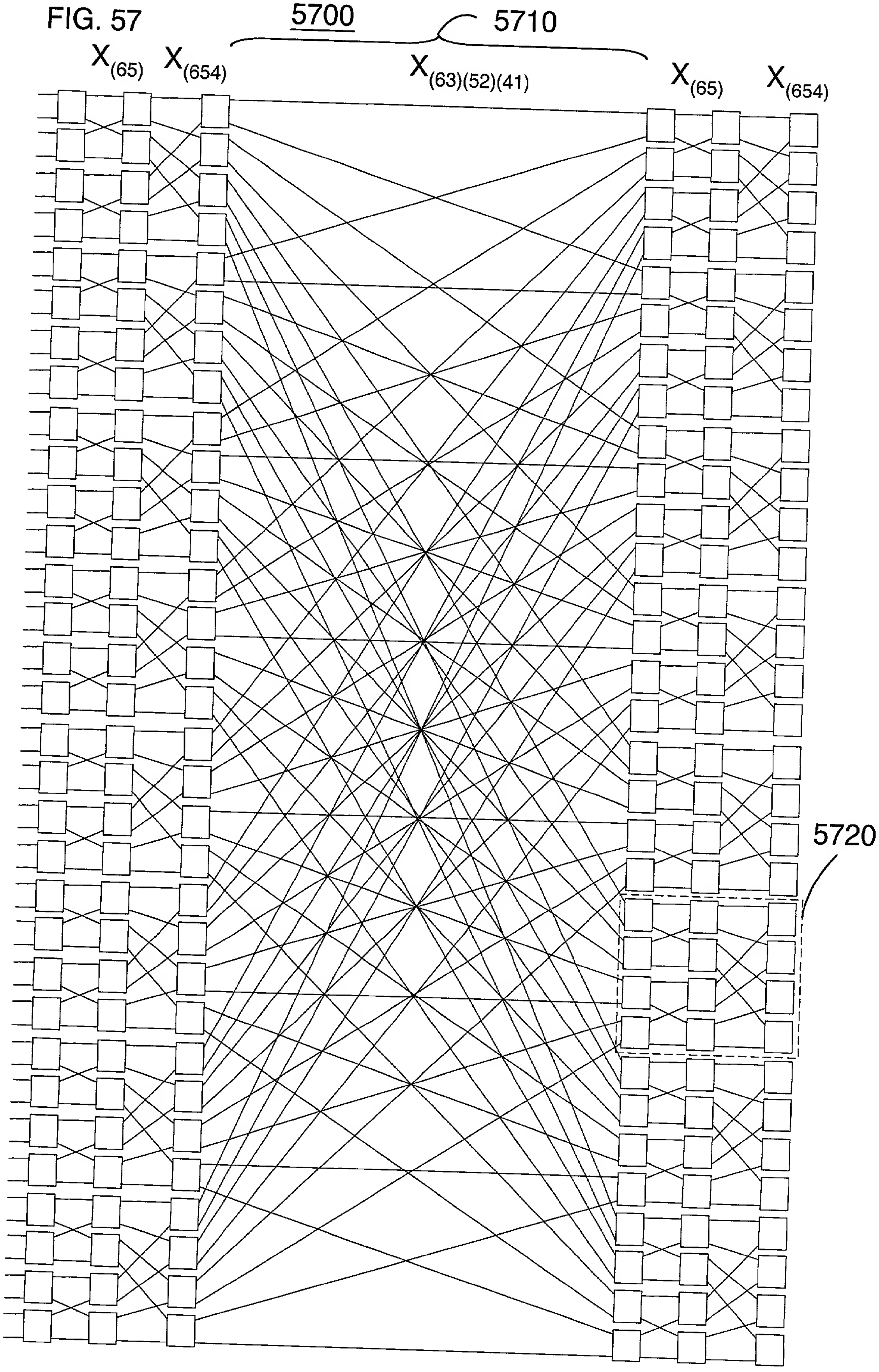


FIG. 58

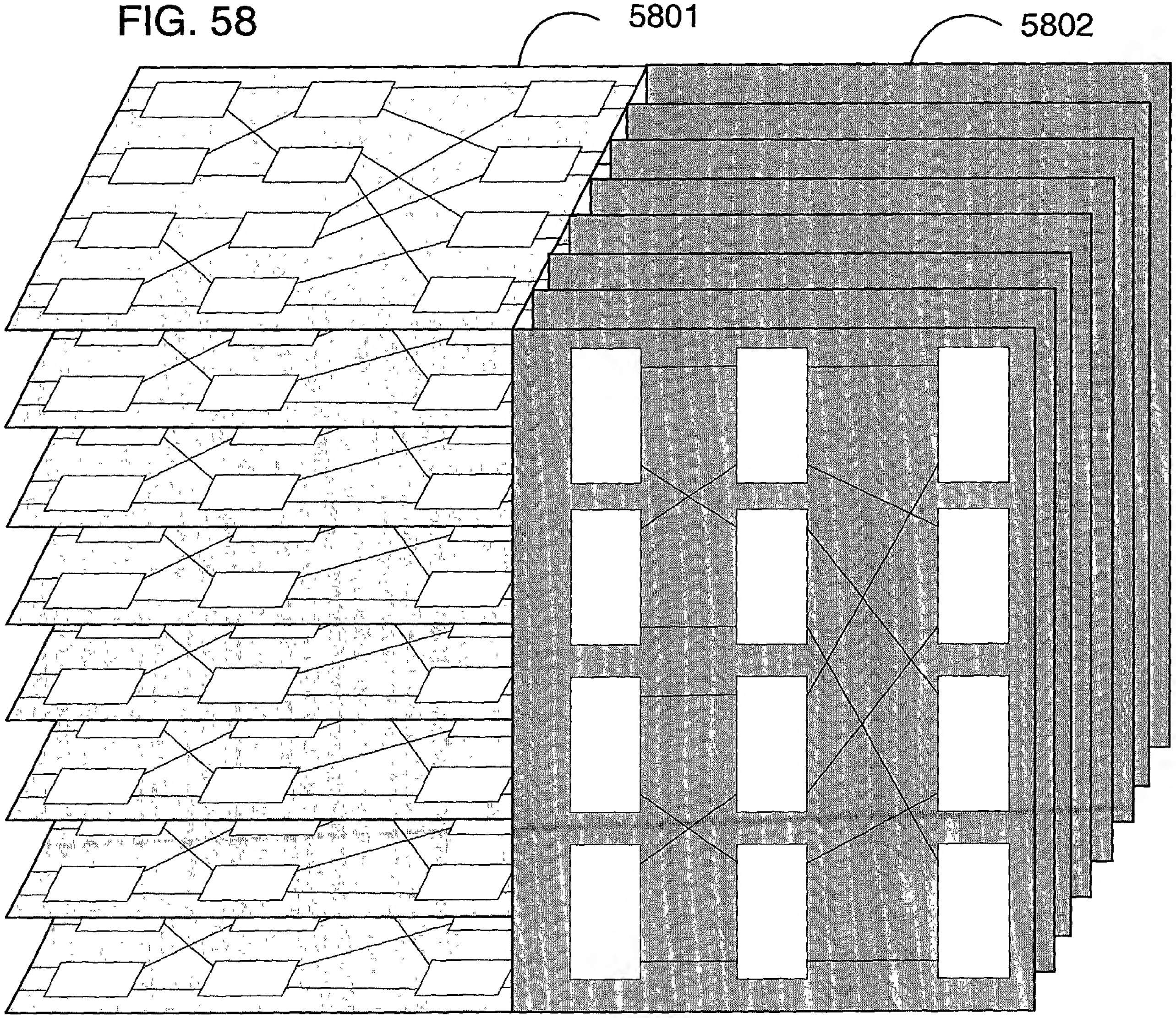
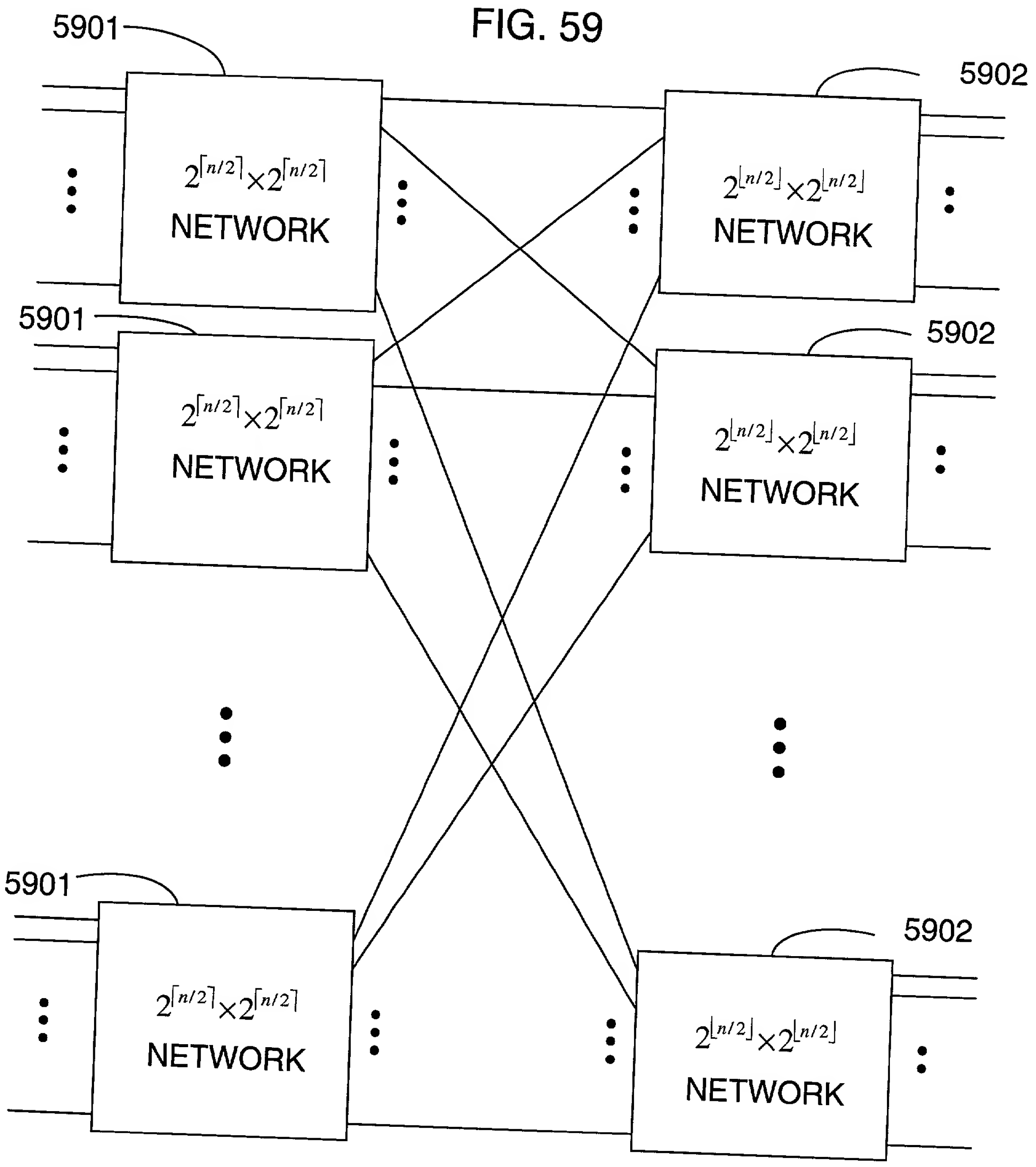


FIG. 59



5901
5901
5901
5902
5902
5902
$2^{\lceil n/2 \rceil} \times 2^{\lceil n/2 \rceil}$ NETWORK
$2^{\lceil n/2 \rceil} \times 2^{\lceil n/2 \rceil}$ NETWORK
$2^{\lceil n/2 \rceil} \times 2^{\lceil n/2 \rceil}$ NETWORK
$2^{\lfloor n/2 \rfloor} \times 2^{\lfloor n/2 \rfloor}$ NETWORK
$2^{\lfloor n/2 \rfloor} \times 2^{\lfloor n/2 \rfloor}$ NETWORK
$2^{\lfloor n/2 \rfloor} \times 2^{\lfloor n/2 \rfloor}$ NETWORK

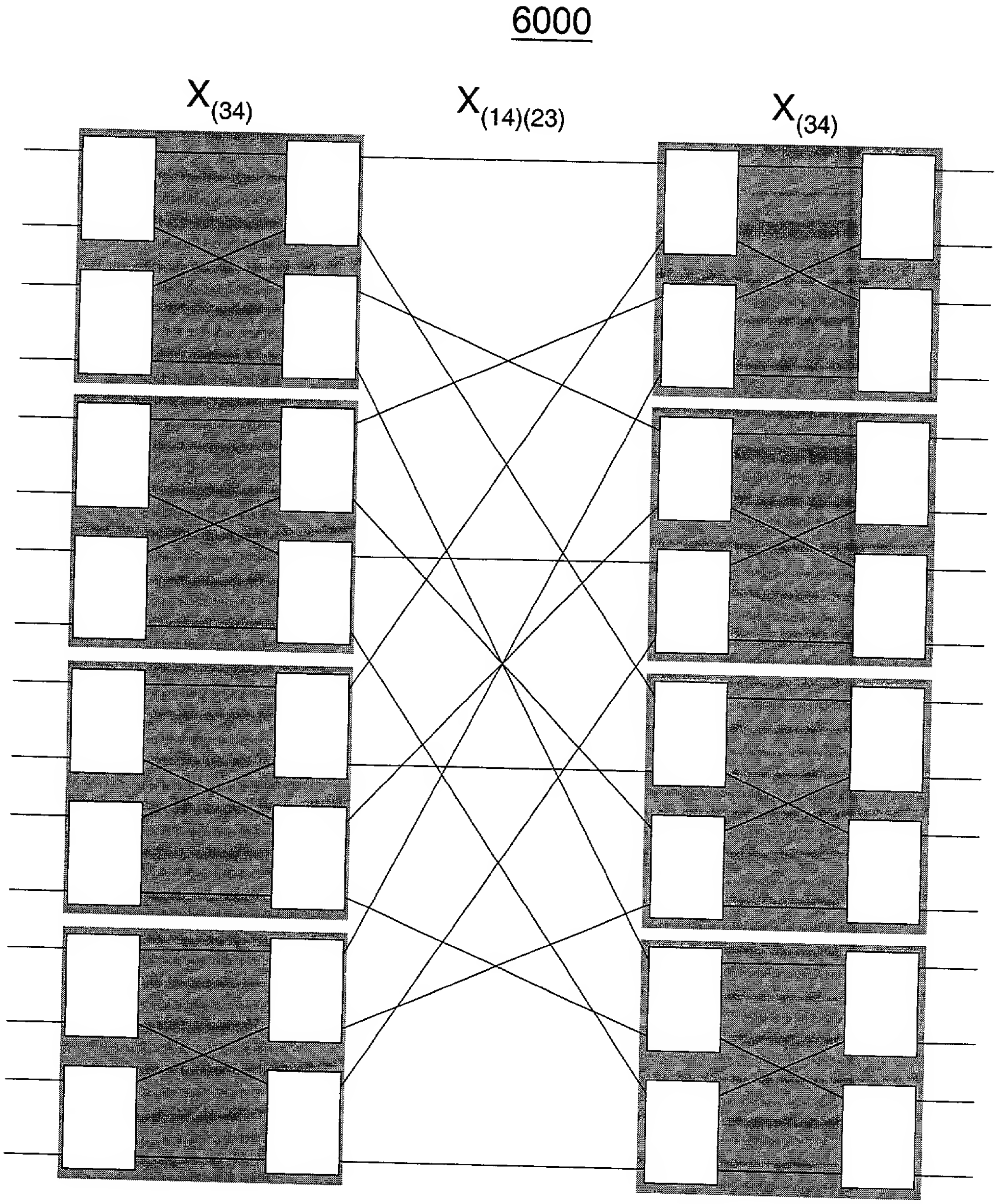
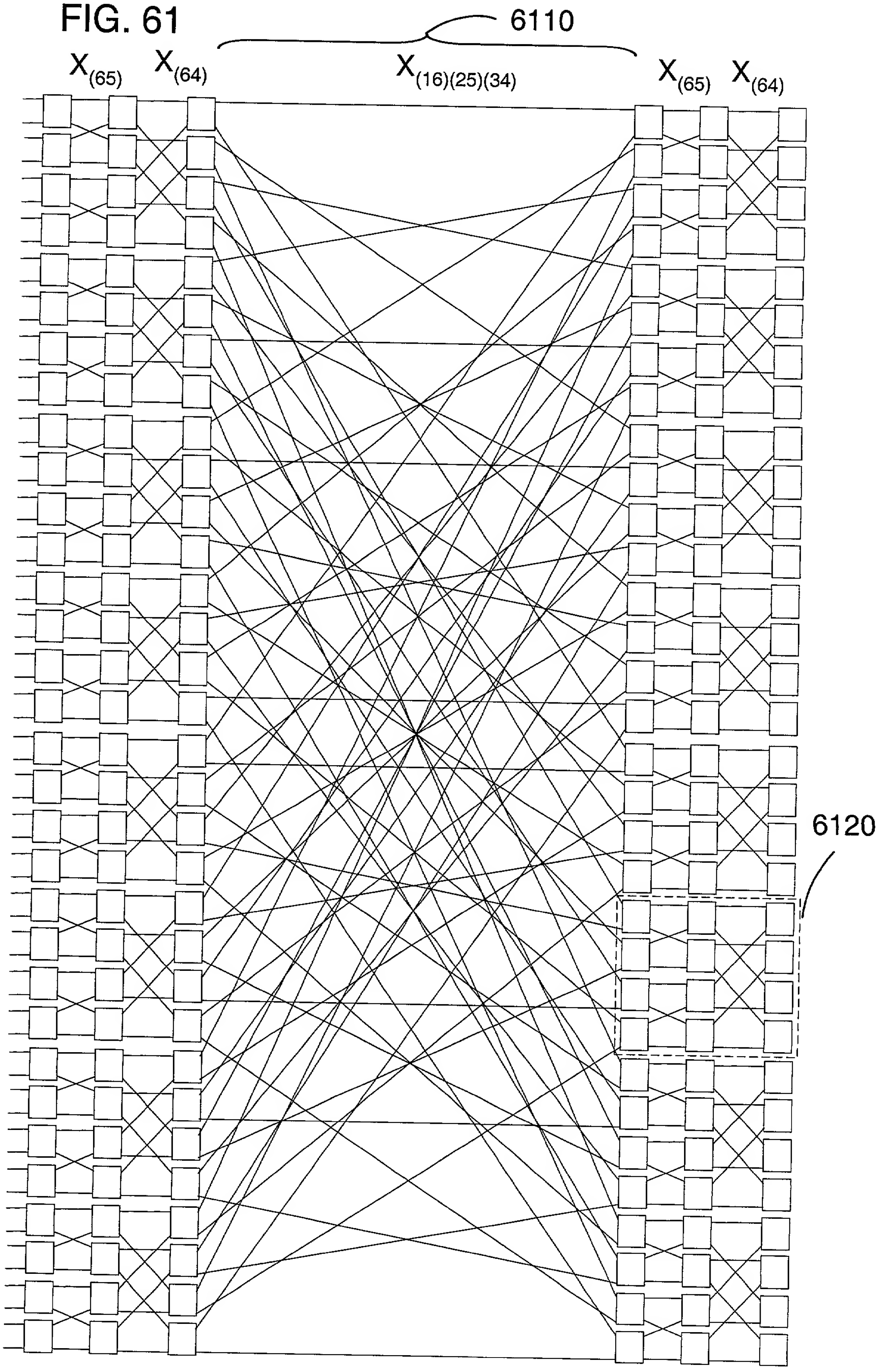


FIG. 60

FIG. 61



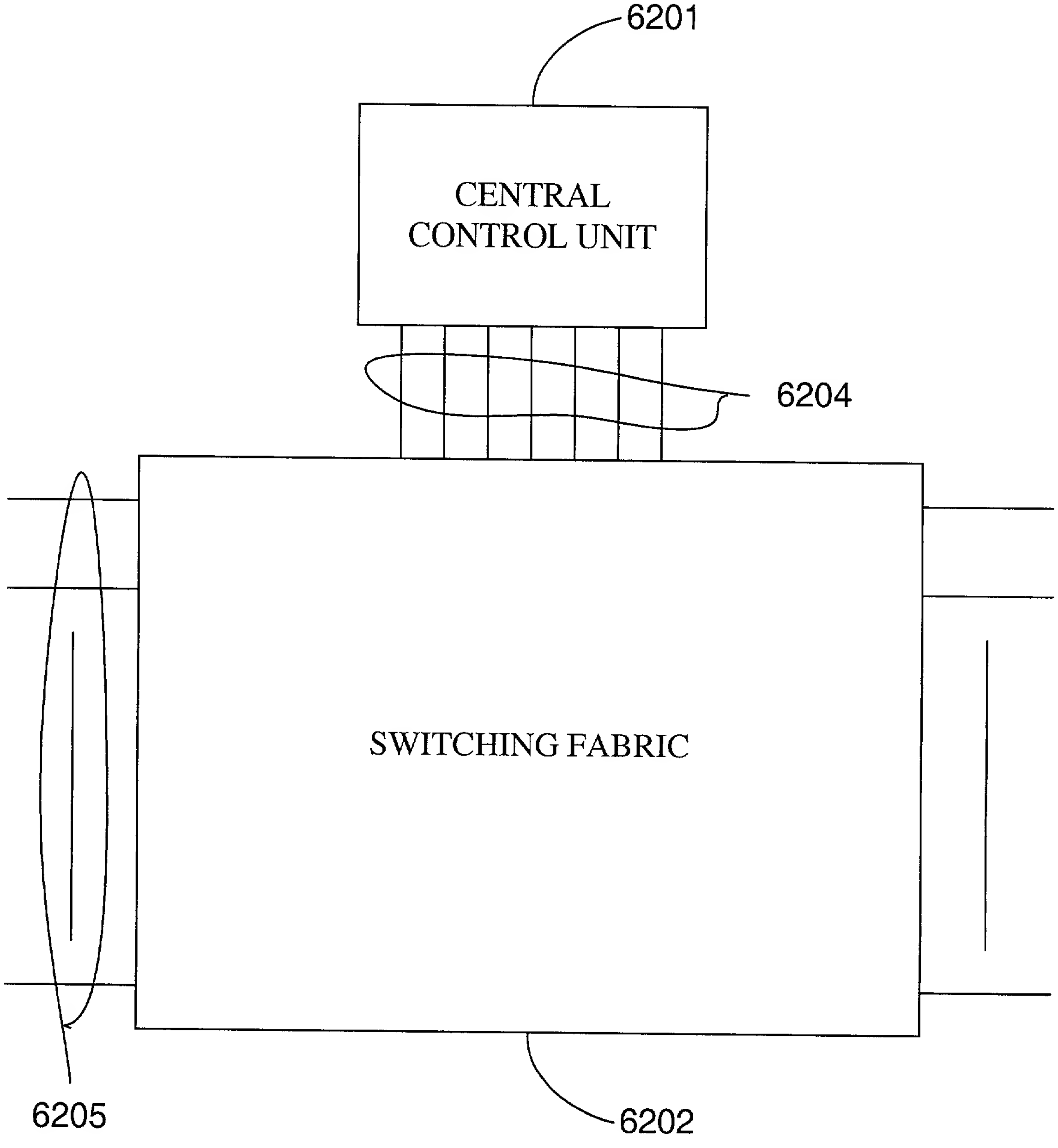


FIG. 62A

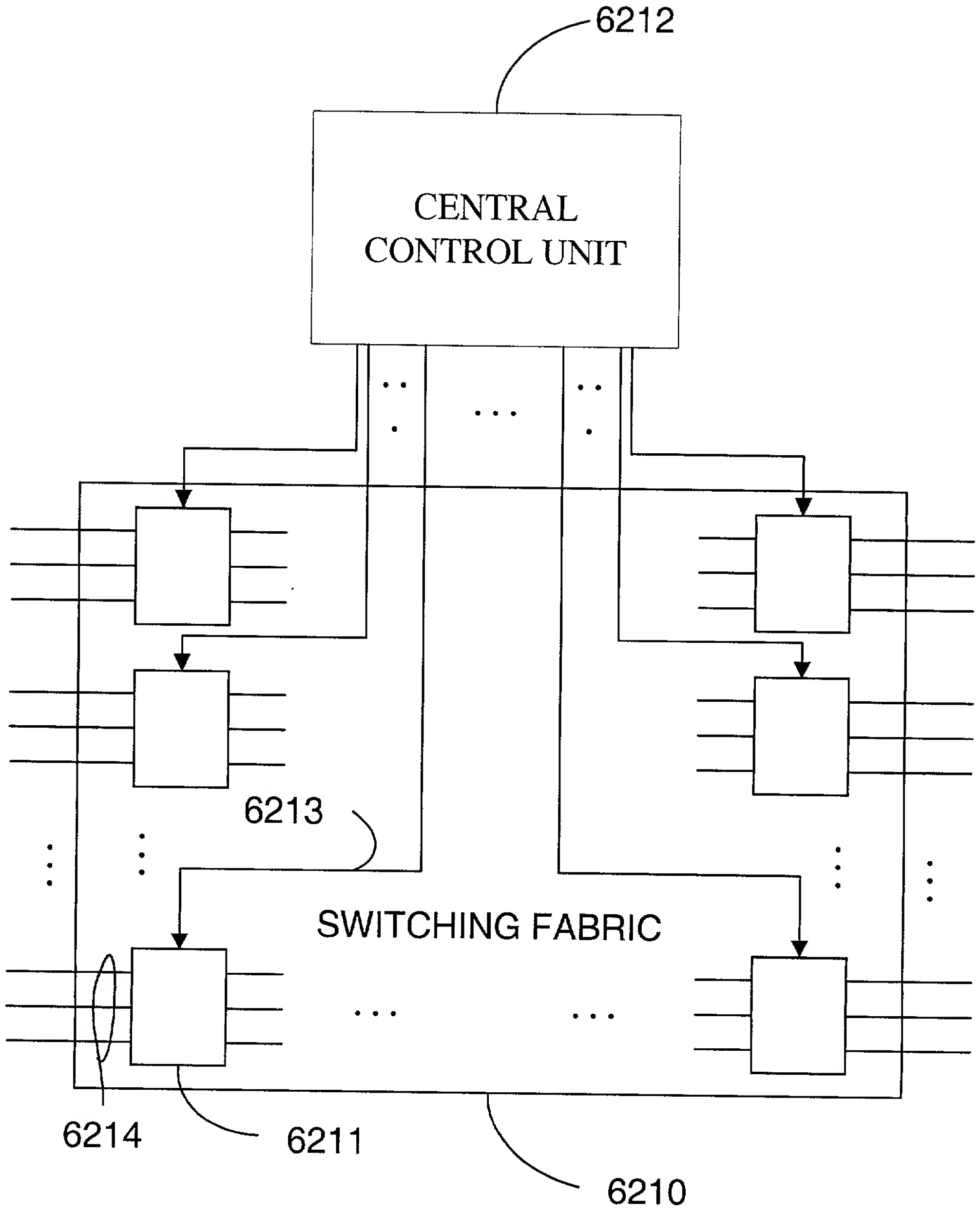

6212
CENTRAL CONTROL UNIT
6213
SWITCHING FABRIC
6214
6211
6210

FIG. 62B

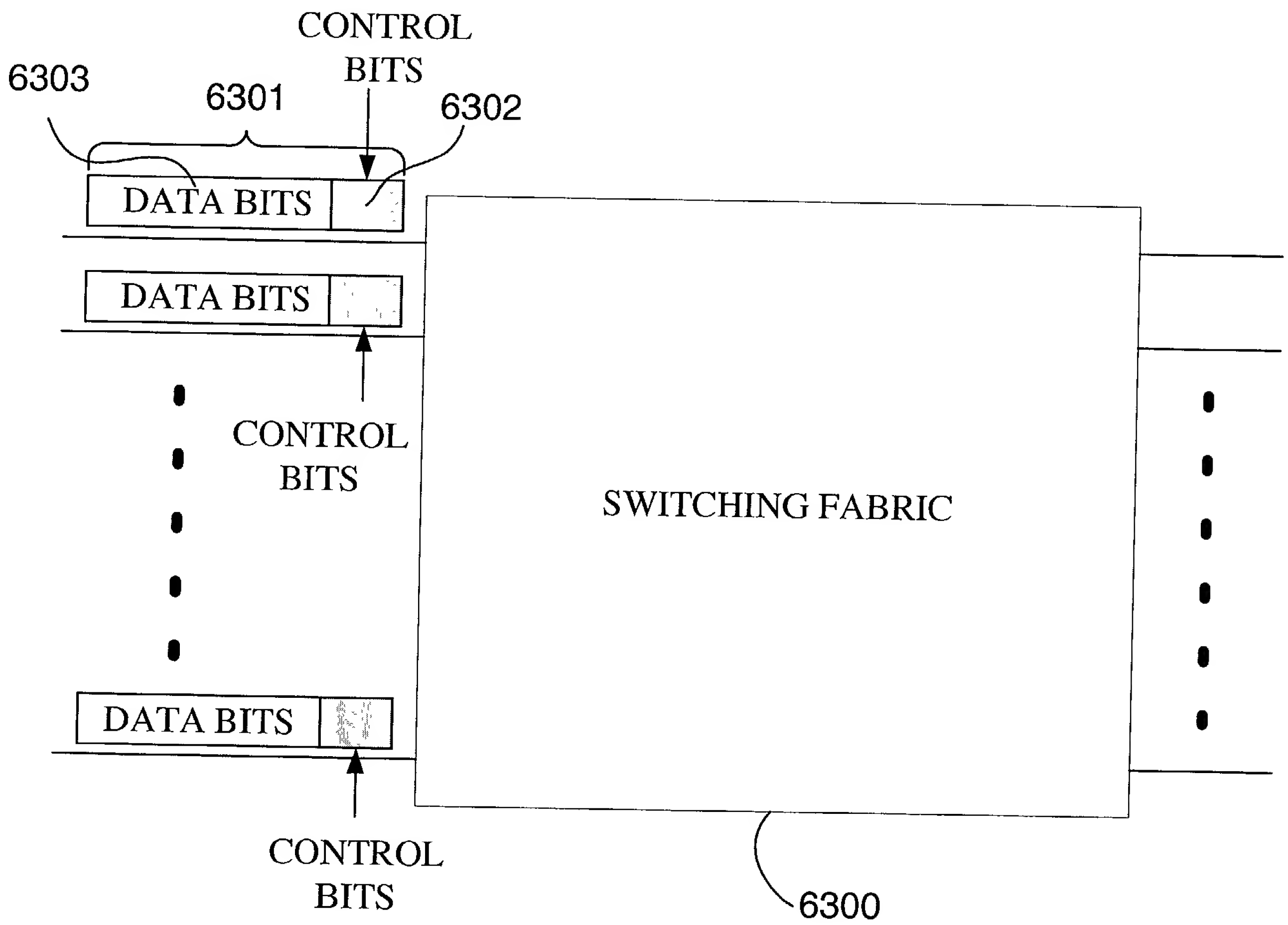

CONTROL BITS
6303
6301
6302
DATA BITS
DATA BITS
CONTROL BITS
DATA BITS
CONTROL BITS
SWITCHING FABRIC
6300

FIG. 63A

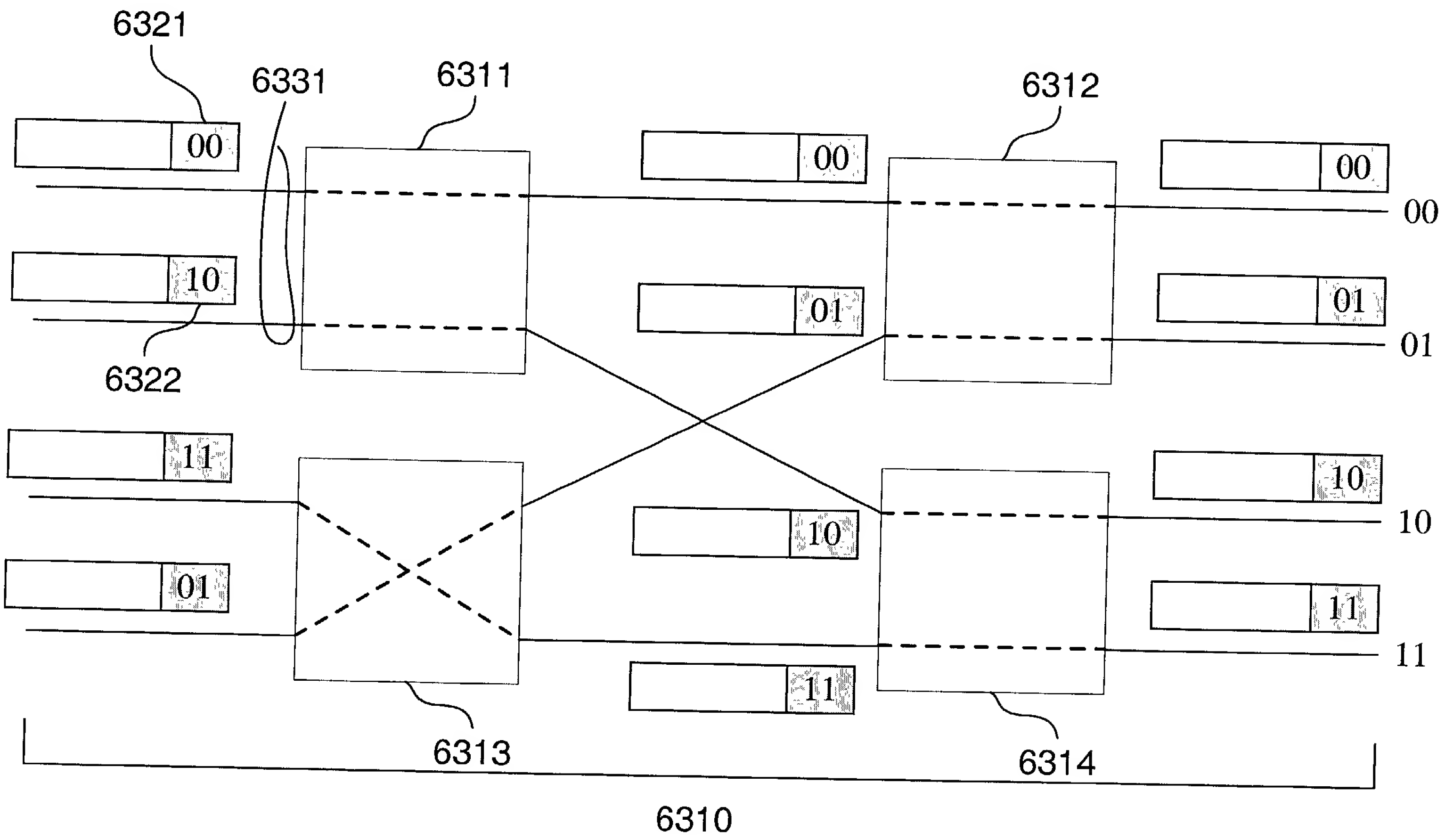

6321
6331
6311
6312
00
10
6322
11
01
00
01
10
11
00
01
10
11
00
01
10
11
6313
6314
6310

FIG. 63B

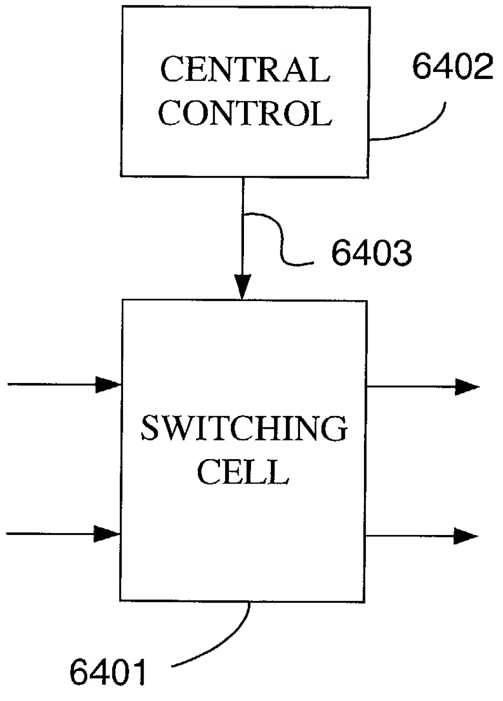


FIG. 64A

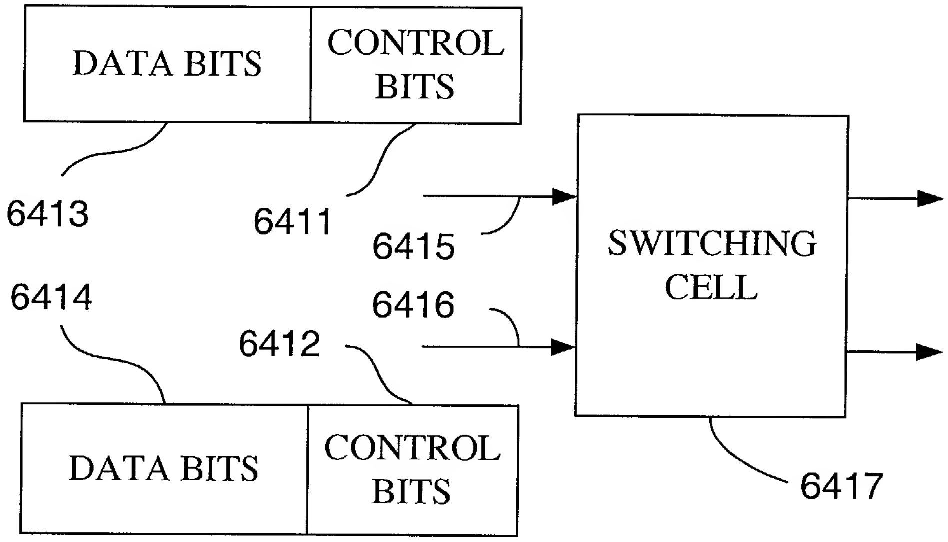


FIG. 64B

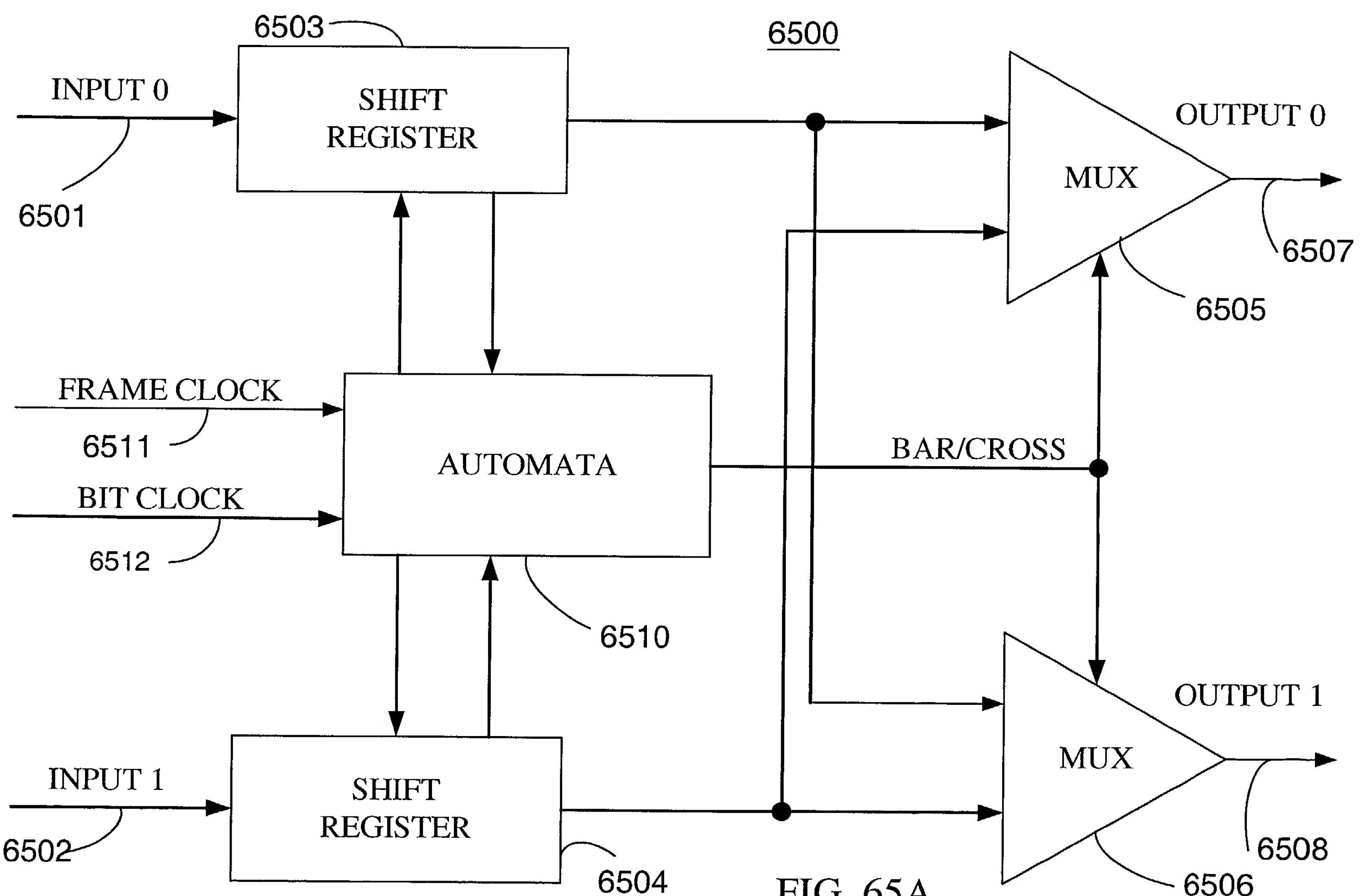

6500
INPUT 0
6501
6503
SHIFT REGISTER
FRAME CLOCK
6511
BIT CLOCK
6512
AUTOMATA
6510
INPUT 1
6502
SHIFT REGISTER
6504
BAR/CROSS
MUX
OUTPUT 0
6505
6507
MUX
OUTPUT 1
6506
6508

FIG. 65A

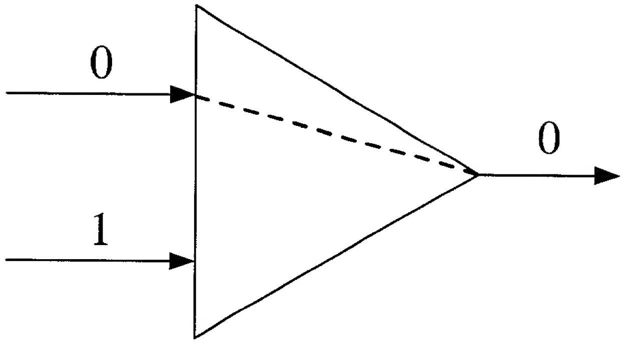


FIG. 65B

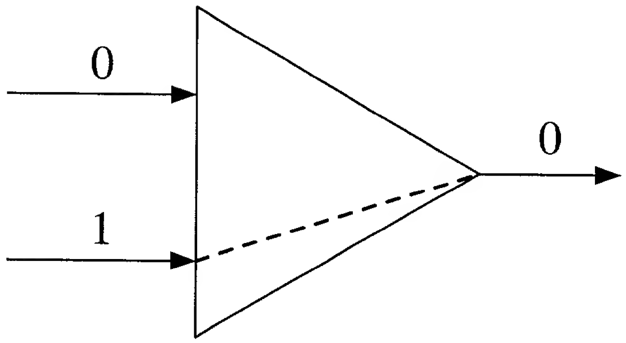


FIG. 65C

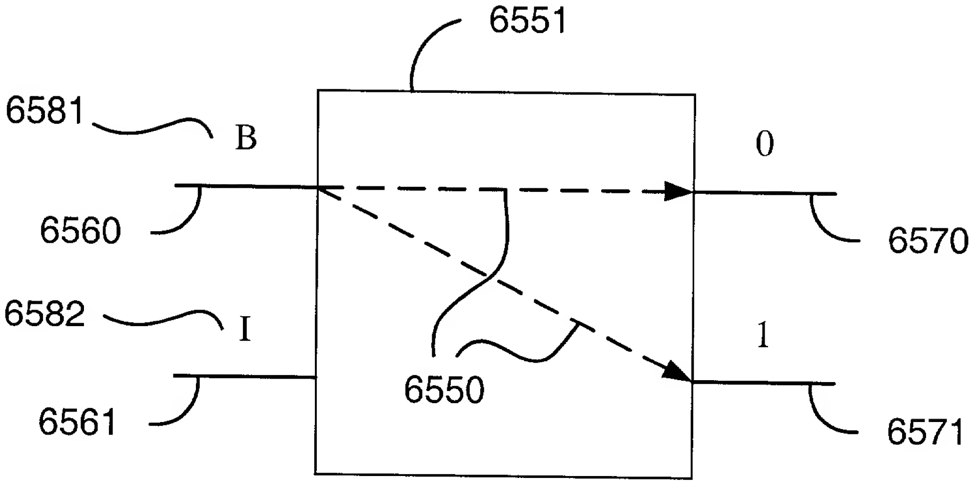


FIG. 65D

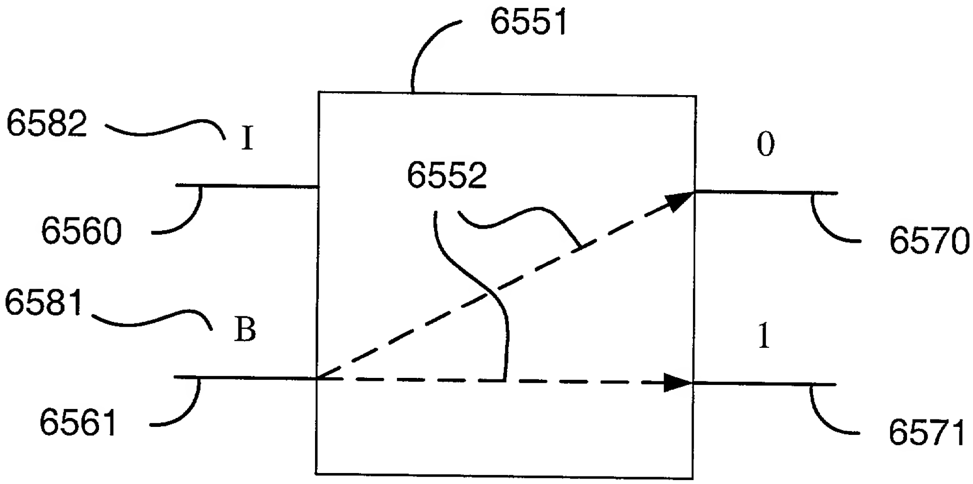


FIG. 65E

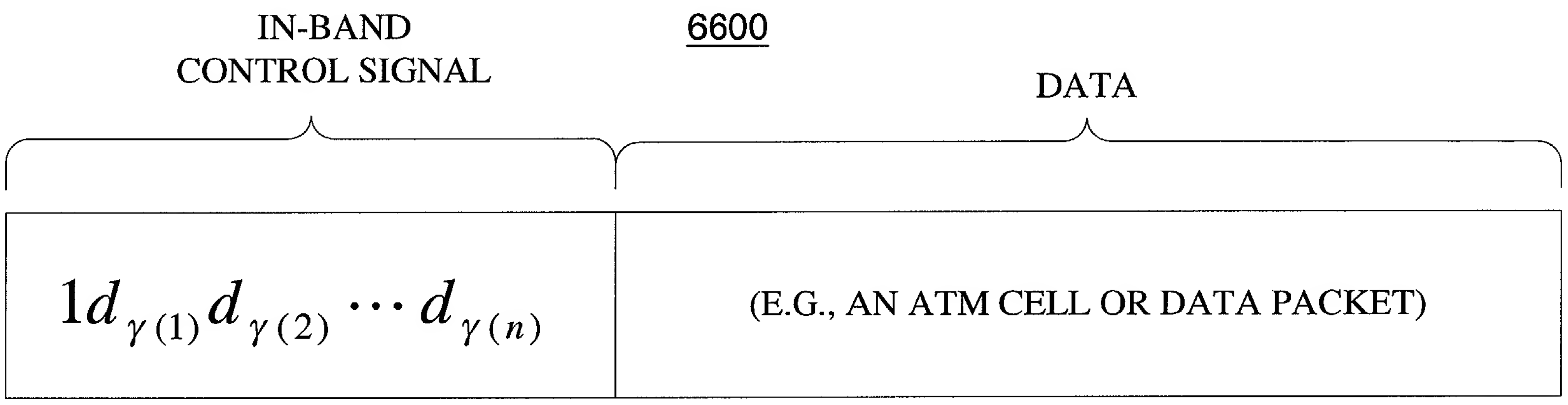

IN-BAND
CONTROL SIGNAL
6600
DATA
$1d_{\gamma(1)}d_{\gamma(2)}\cdots d_{\gamma(n)}$
(E.G., AN ATM CELL OR DATA PACKET)

FIG. 66A

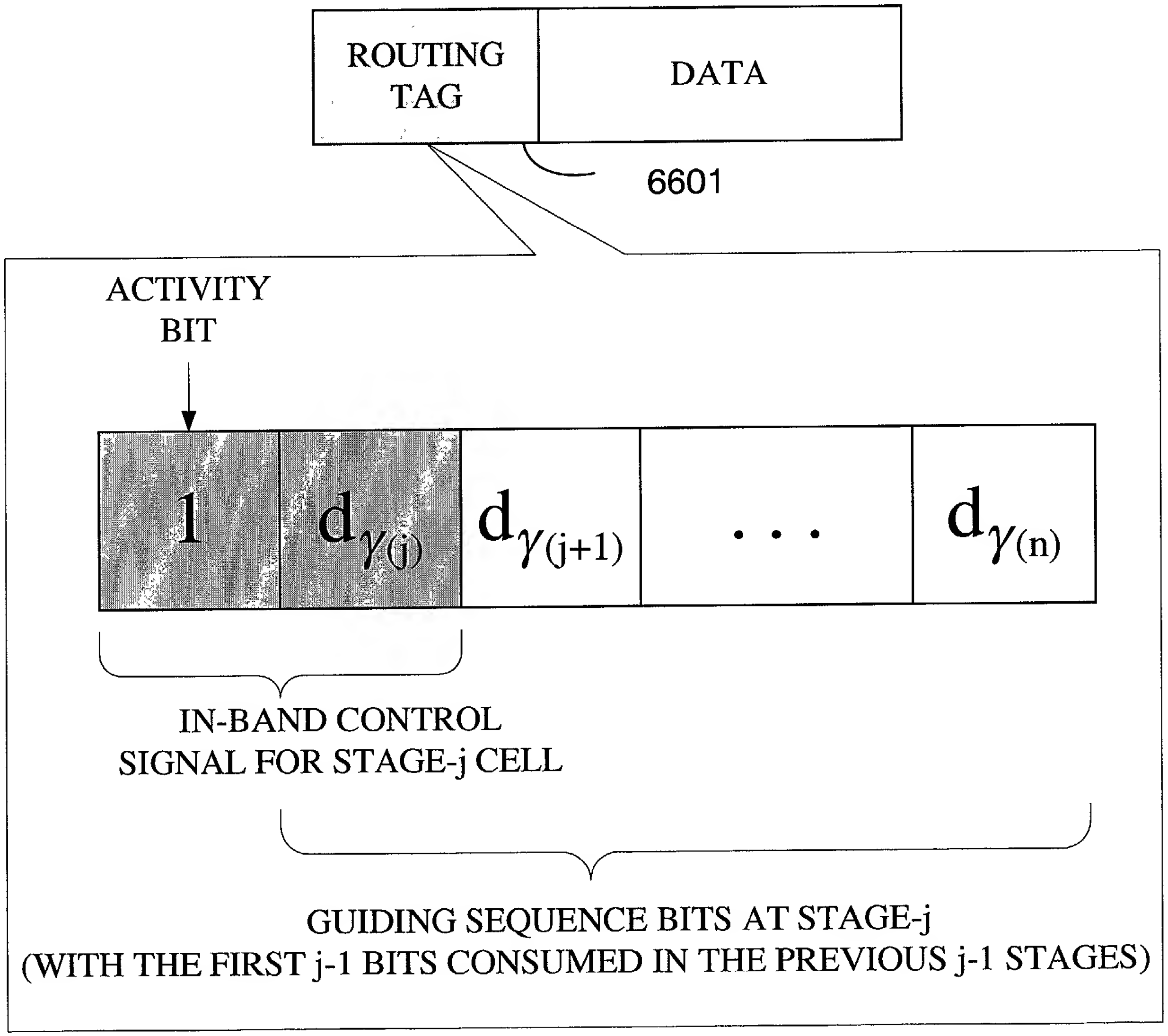

ROUTING TAG
DATA
6601
ACTIVITY BIT
1
$d_{\gamma(j)}$
$d_{\gamma(j+1)}$
. . .
$d_{\gamma(n)}$
IN-BAND CONTROL SIGNAL FOR STAGE-j CELL
GUIDING SEQUENCE BITS AT STAGE-j
(WITH THE FIRST j-1 BITS CONSUMED IN THE PREVIOUS j-1 STAGES)

FIG. 66B

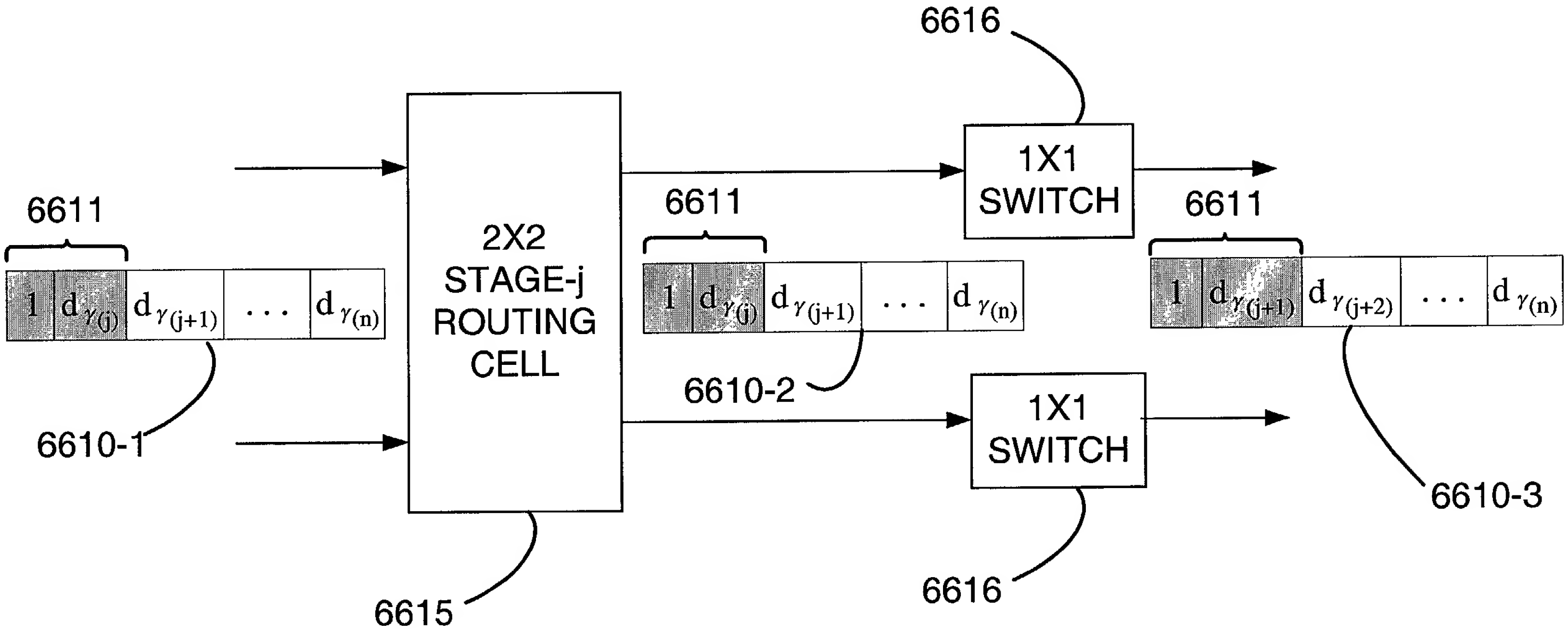

6611
1
$d_{\gamma(j)}$
$d_{\gamma(j+1)}$
. . .
$d_{\gamma(n)}$
6610-1
2X2
STAGE-j
ROUTING
CELL
6615
6611
1
$d_{\gamma(j)}$
$d_{\gamma(j+1)}$
. . .
$d_{\gamma(n)}$
6610-2
6616
1X1
SWITCH
1X1
SWITCH
6616
6611
1
$d_{\gamma(j+1)}$
$d_{\gamma(j+2)}$
. . .
$d_{\gamma(n)}$
6610-3

FIG. 66C

FIG. 66D

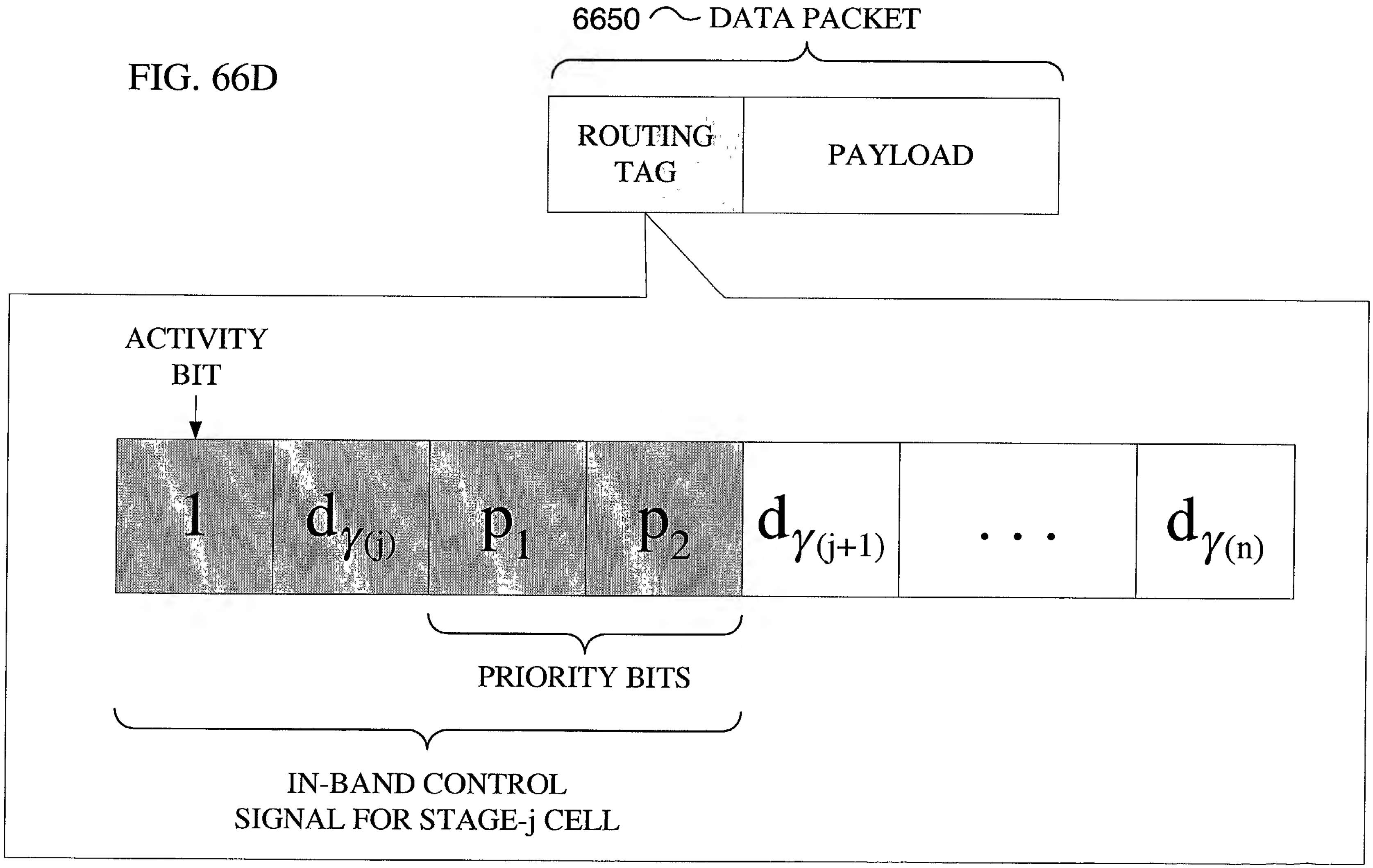

6650
DATA PACKET
ROUTING TAG
PAYLOAD
ACTIVITY BIT
1
$d_{\gamma(j)}$
p_1
p_2
$d_{\gamma(j+1)}$
. . .
$d_{\gamma(n)}$
PRIORITY BITS
IN-BAND CONTROL SIGNAL FOR STAGE-j CELL

FIG. 67A

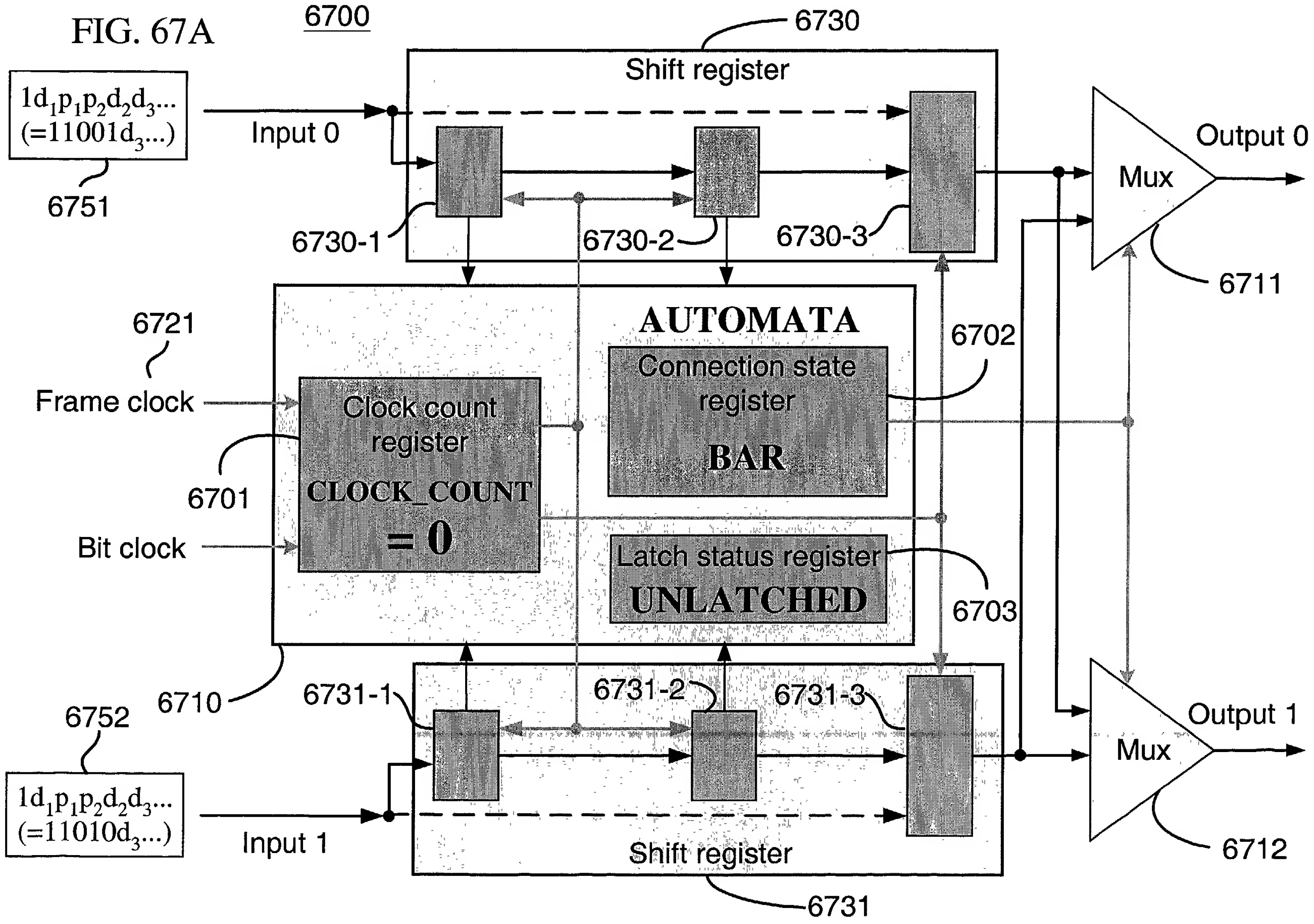

6700
6730
Shift register
$1d_1p_1p_2d_2d_3\ldots$
$(=11001d_3\ldots)$
Input 0
6751
6730-1
6730-2
6730-3
Mux
Output 0
6711
AUTOMATA
6721
Frame clock
Clock count register
CLOCK_COUNT
= 0
6701
Bit clock
Connection state register
BAR
6702
Latch status register
UNLATCHED
6703
6710
6752
6731-1
6731-2
6731-3
Output 1
Mux
6712
$1d_1p_1p_2d_2d_3\ldots$
$(=11010d_3\ldots)$
Input 1
Shift register
6731

FIG. 67B

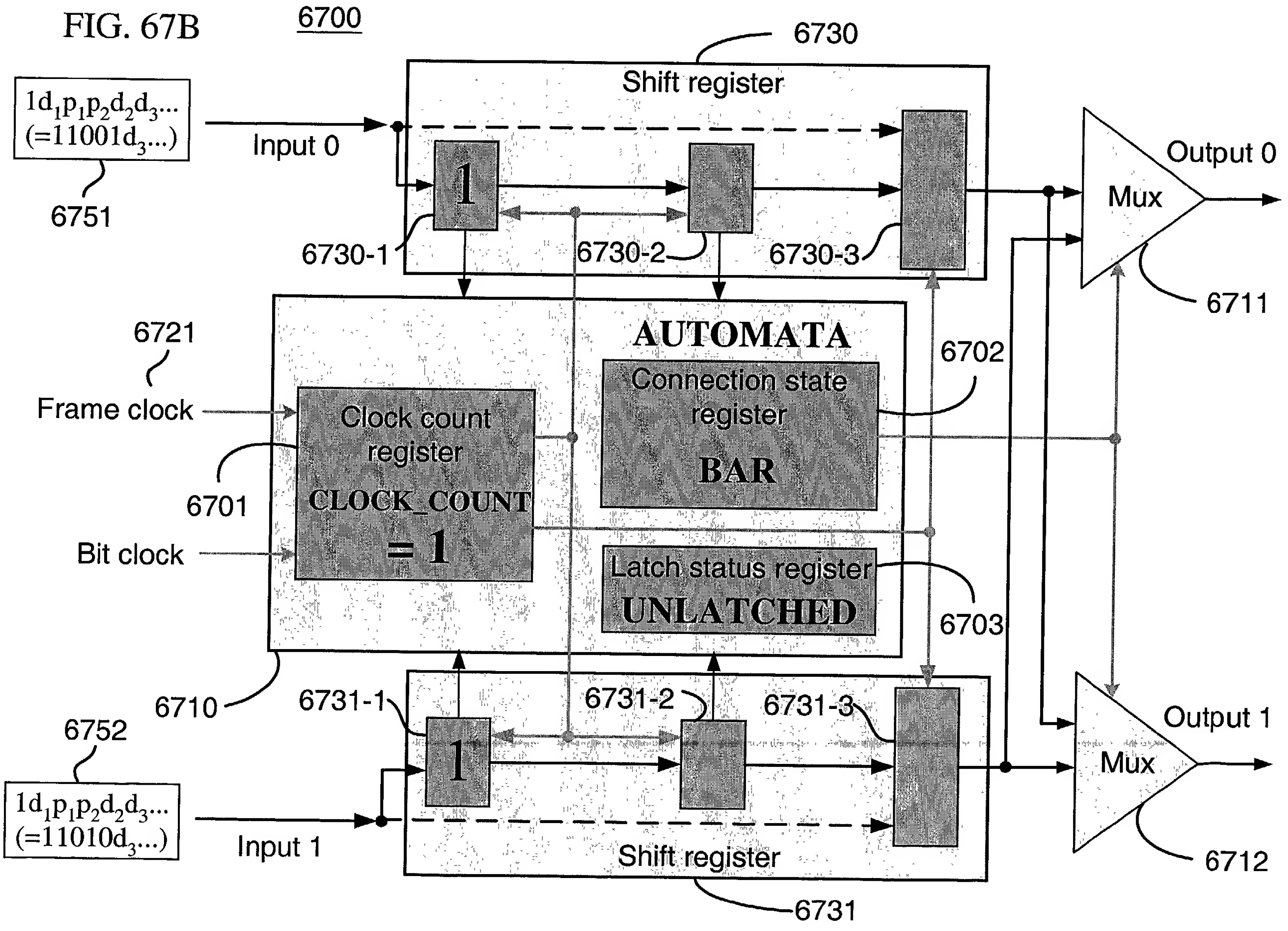

6700
6730
Shift register
$1d_1p_1p_2d_2d_3$...
(=$11001d_3$...)
6751
Input 0
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
6721
Frame clock
6701
Bit clock
AUTOMATA
Clock count register
CLOCK_COUNT
= 1
Connection state register
BAR
Latch status register
UNLATCHED
6702
6703
6710
6752
$1d_1p_1p_2d_2d_3$...
(=$11010d_3$...)
Input 1
6731-1
1
6731-2
6731-3
Shift register
6731
Output 1
Mux
6712

FIG. 67C

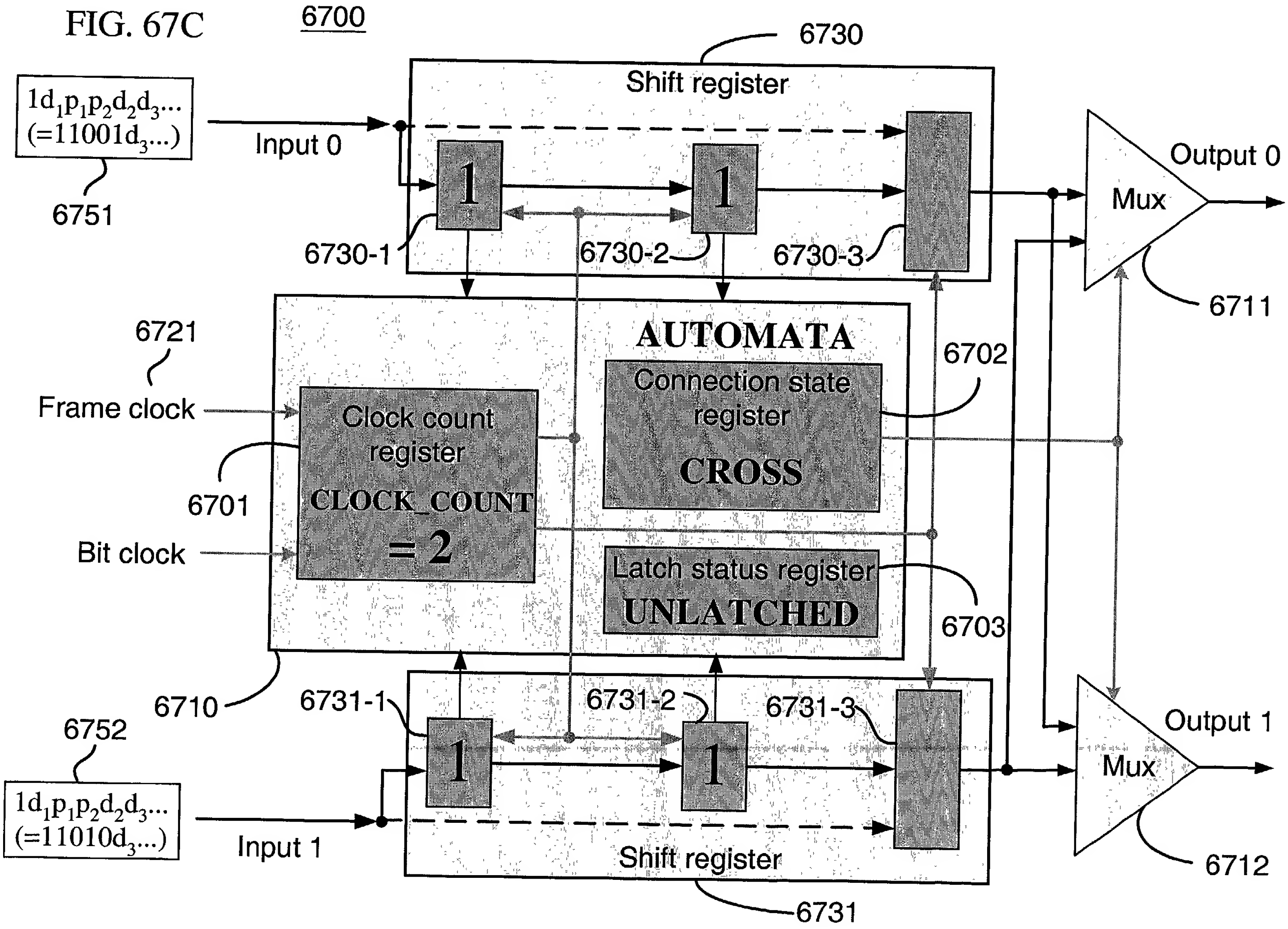
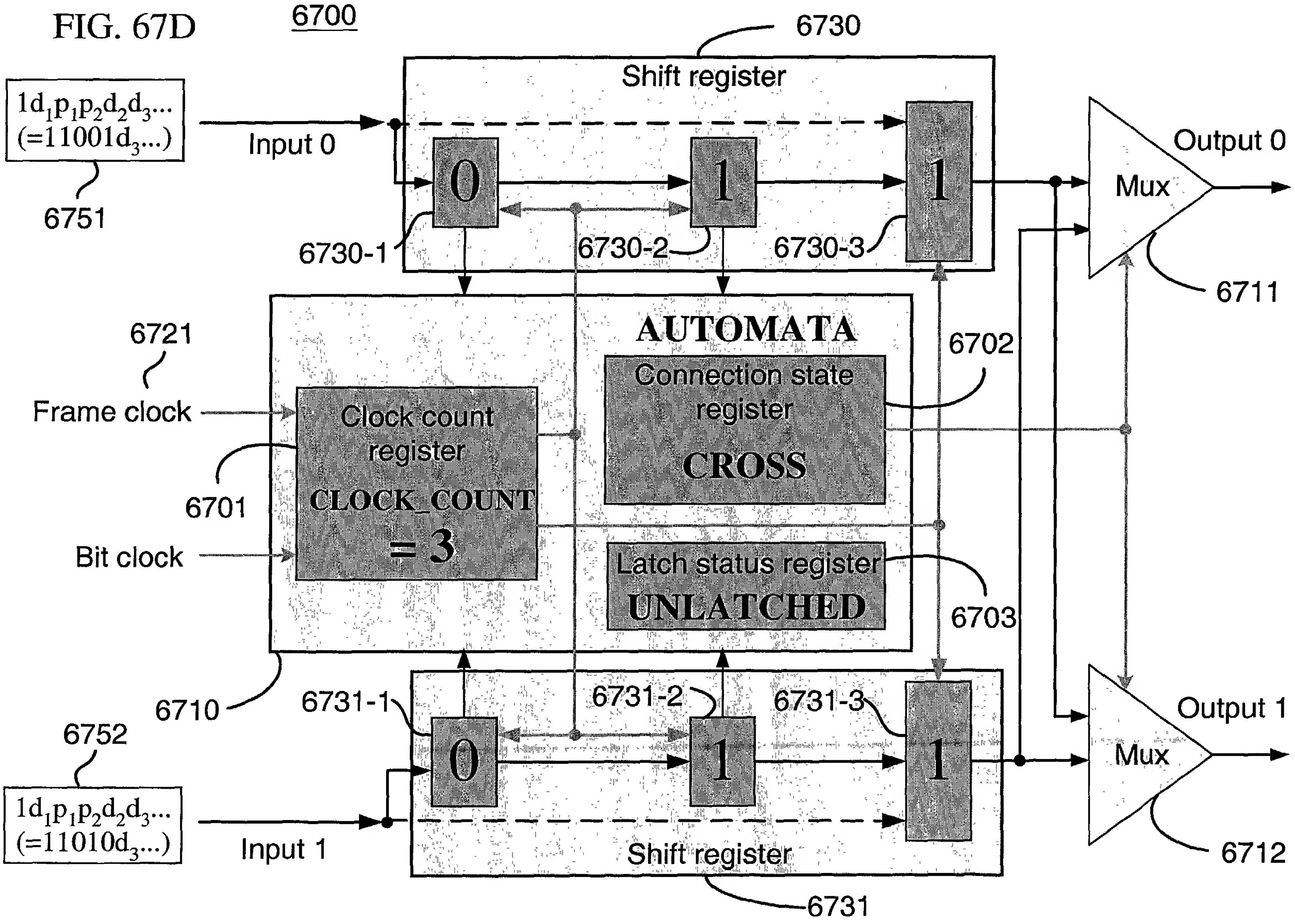

6700
6730
Shift register
$1d_1p_1p_2d_2d_3...$
$(=11001d_3...)$
6751
Input 0
1
1
6730-1
6730-2
6730-3
Mux
Output 0
6711
AUTOMATA
6702
Connection state register
CROSS
6721
Frame clock
Clock count register
CLOCK_COUNT
= 2
6701
Bit clock
Latch status register
UNLATCHED
6703
6710
6752
6731-1
6731-2
6731-3
1
1
Mux
Output 1
$1d_1p_1p_2d_2d_3...$
$(=11010d_3...)$
Input 1
Shift register
6712
6731

FIG. 67D



6700
6730
Shift register
$1d_1p_1p_2d_2d_3\ldots$ $(=11001d_3\ldots)$
6751
Input 0
0
1
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
6721
Frame clock
AUTOMATA
Connection state register
CROSS
6702
Clock count register
CLOCK_COUNT = 3
6701
Bit clock
Latch status register
UNLATCHED
6703
6710
6731-1
6731-2
6731-3
6752
$1d_1p_1p_2d_2d_3\ldots$ $(=11010d_3\ldots)$
Input 1
0
1
1
Output 1
Mux
6712
Shift register
6731

FIG. 67E

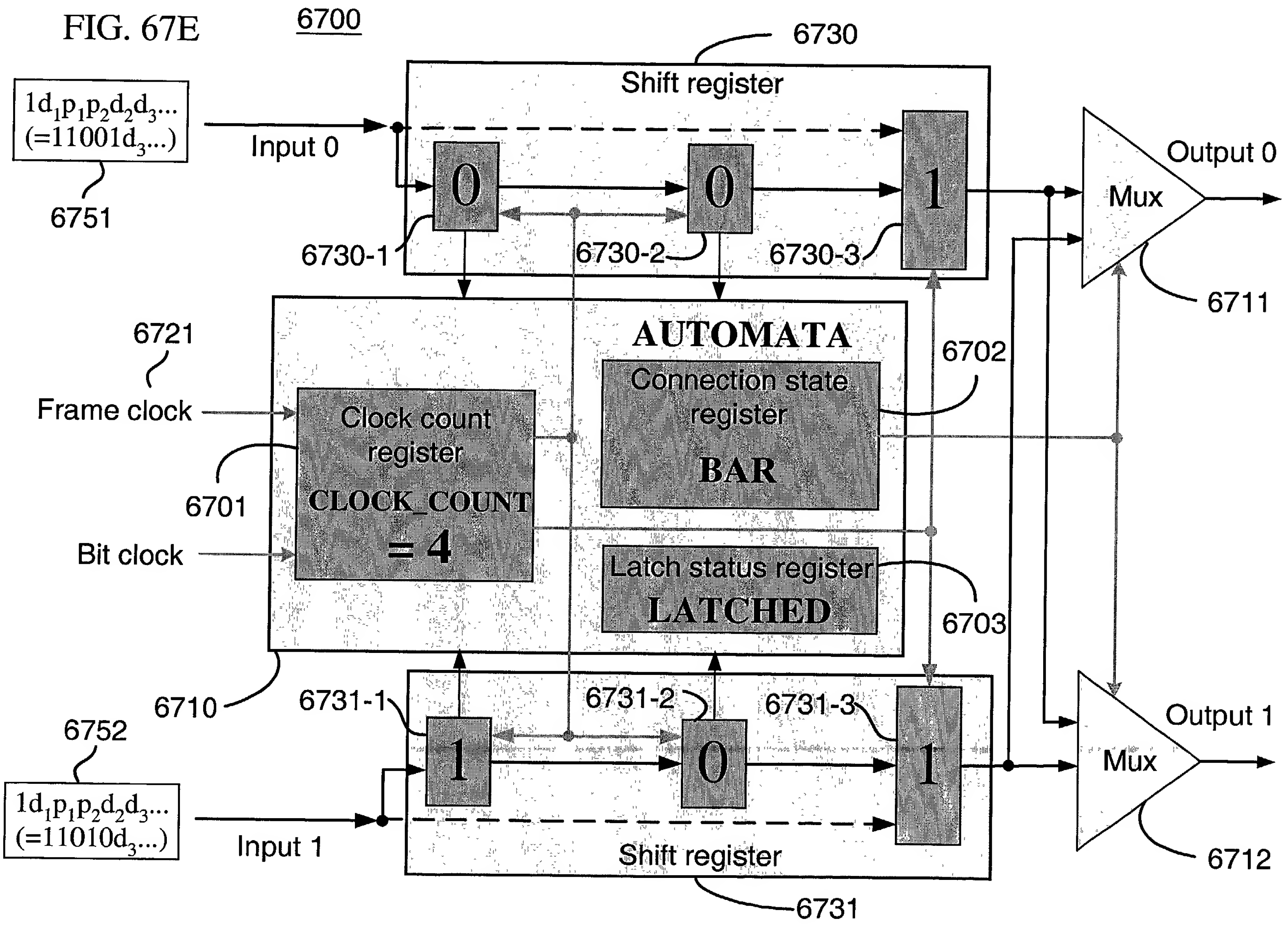
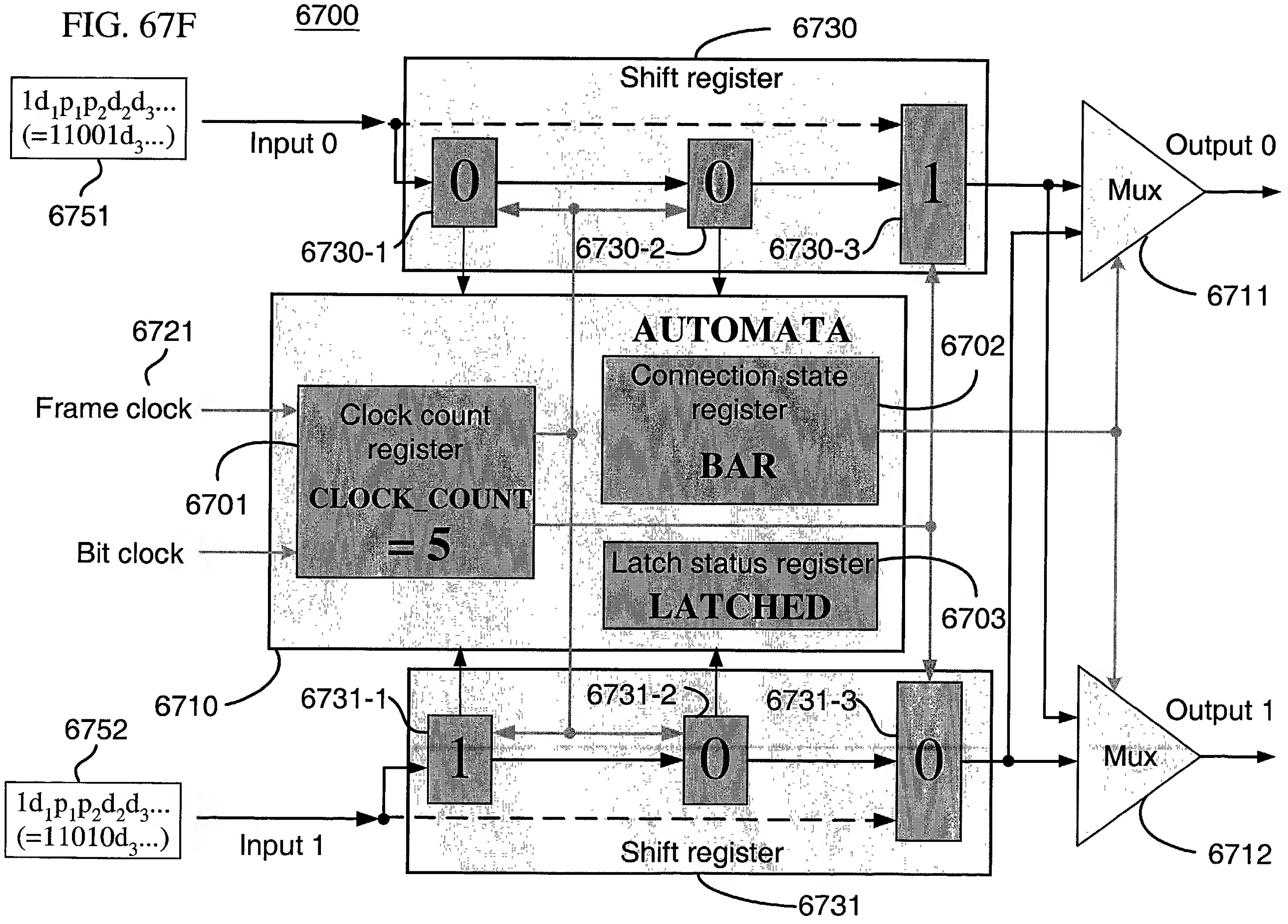

6700
6730
Shift register
$1d_1p_1p_2d_2d_3$...
(=$11001d_3$...)
6751
Input 0
0
0
1
6730-1
6730-2
6730-3
Output 0
Mux
6711
6721
Frame clock
6701
Bit clock
AUTOMATA
Clock count register
CLOCK_COUNT
= 4
Connection state register
BAR
Latch status register
LATCHED
6702
6703
6710
6752
$1d_1p_1p_2d_2d_3$...
(=$11010d_3$...)
Input 1
6731-1
6731-2
6731-3
1
0
1
Shift register
6731
Output 1
Mux
6712

FIG. 67F


6700
6730
Shift register
1d$_1$p$_1$p$_2$d$_2$d$_3$...
(=11001d$_3$...)
6751
Input 0
0
0
1
6730-1
6730-2
6730-3
Mux
Output 0
6711
6721
Frame clock
6701
Bit clock
AUTOMATA
Clock count register
CLOCK_COUNT
= 5
Connection state register
BAR
Latch status register
LATCHED
6702
6703
6710
6752
1d$_1$p$_1$p$_2$d$_2$d$_3$...
(=11010d$_3$...)
Input 1
6731-1
6731-2
6731-3
1
0
0
Shift register
6731
Mux
Output 1
6712

6800

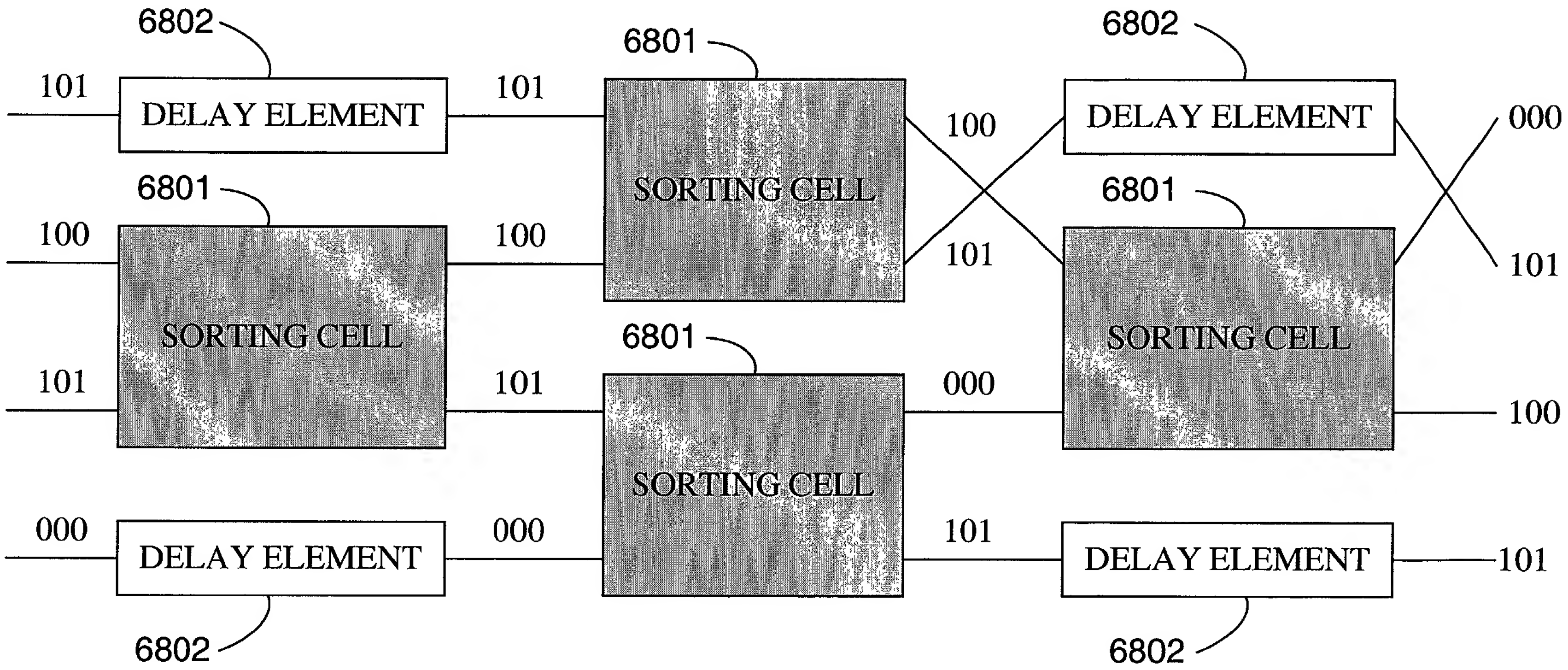
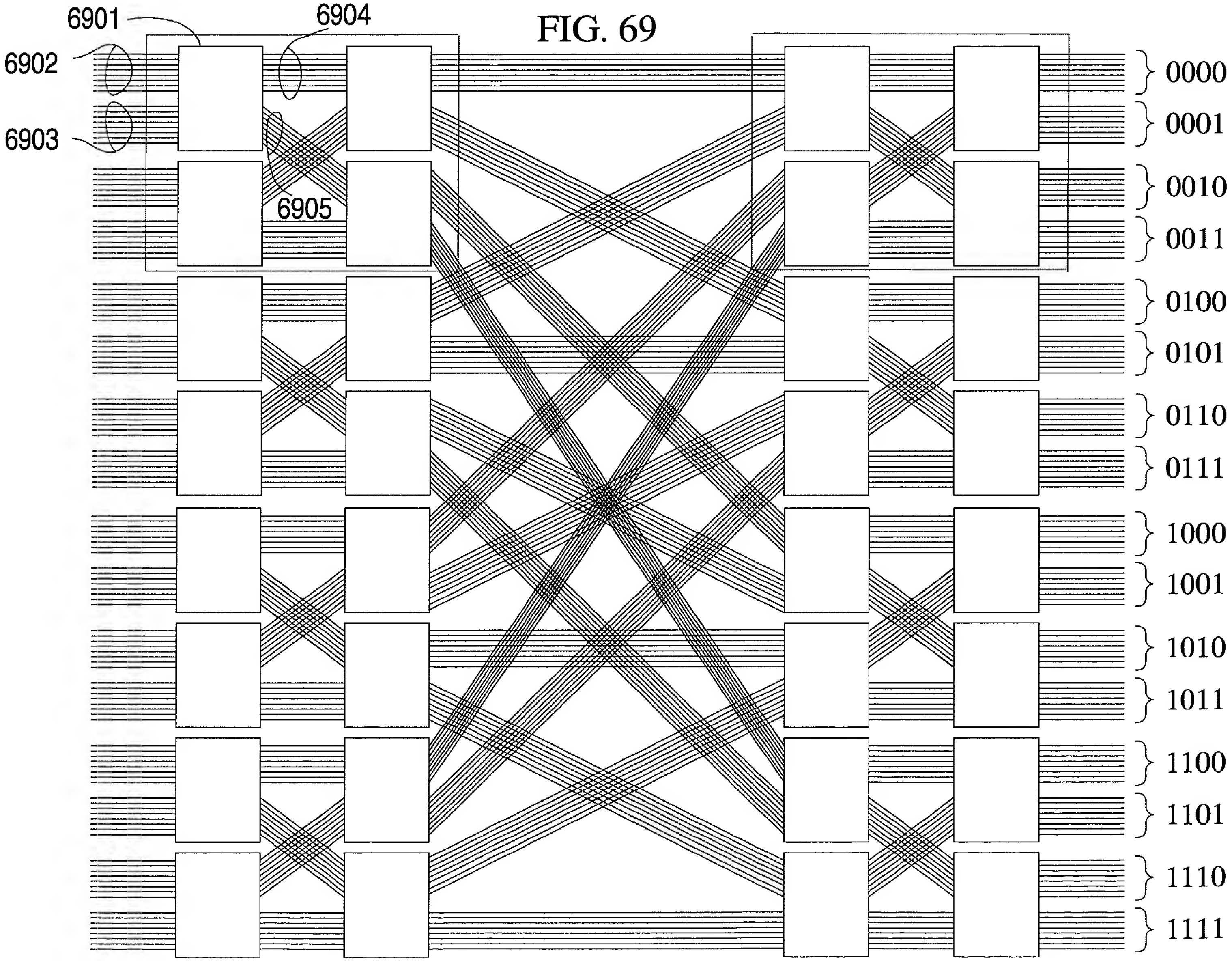

6802
101
DELAY ELEMENT
101
6801
100
SORTING CELL
100
101
101
000
DELAY ELEMENT
000
6802
6801
SORTING CELL
100
101
6801
SORTING CELL
000
101
6802
DELAY ELEMENT
000
101
6801
SORTING CELL
100
DELAY ELEMENT
101
6802

FIG. 68

FIG. 69


6901
6902
6903
6904
6905
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

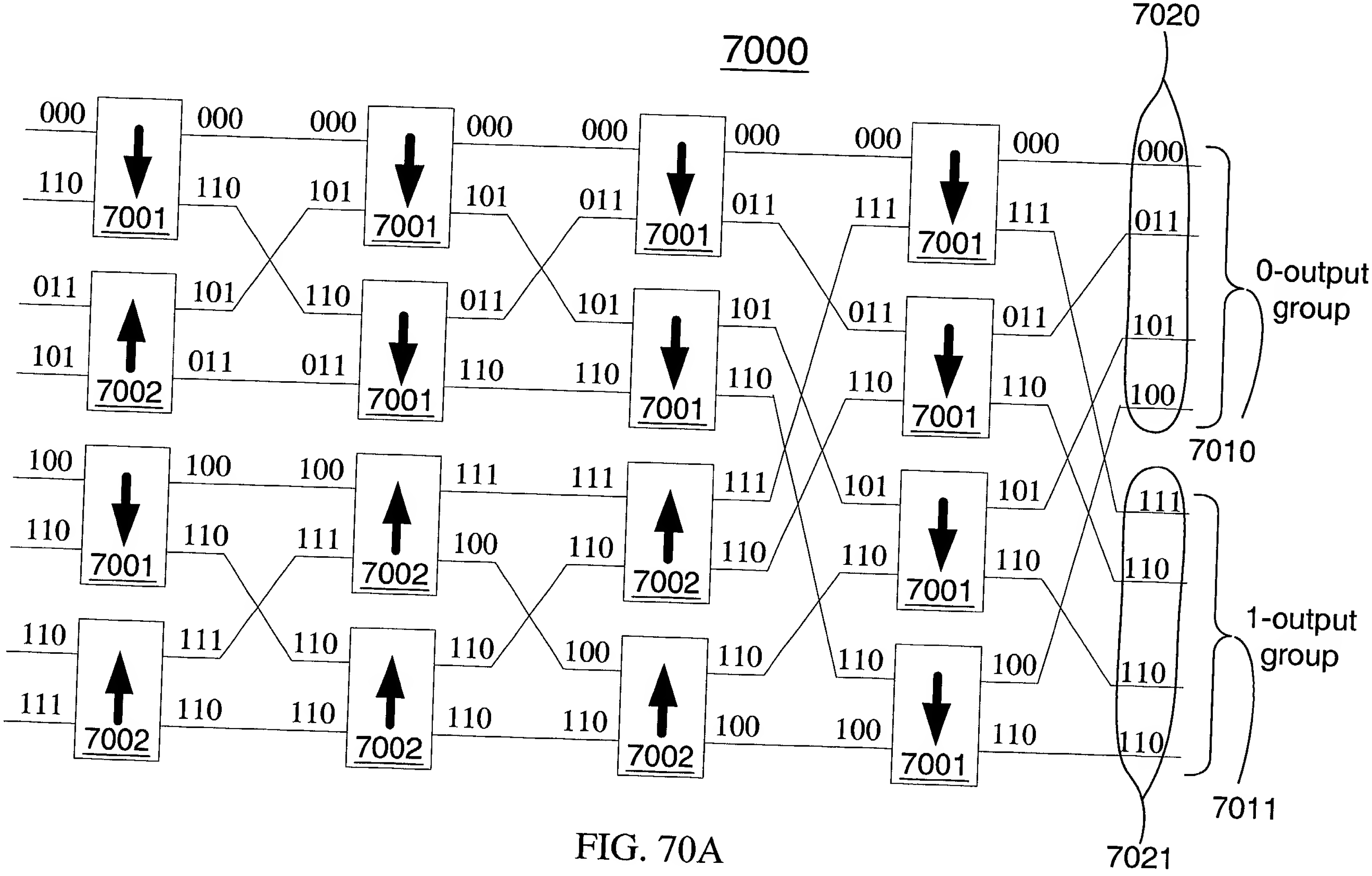

7000
7020
7010
7011
7021
0-output group
1-output group
7001
7002
000
110
011
101
100
111

FIG. 70A

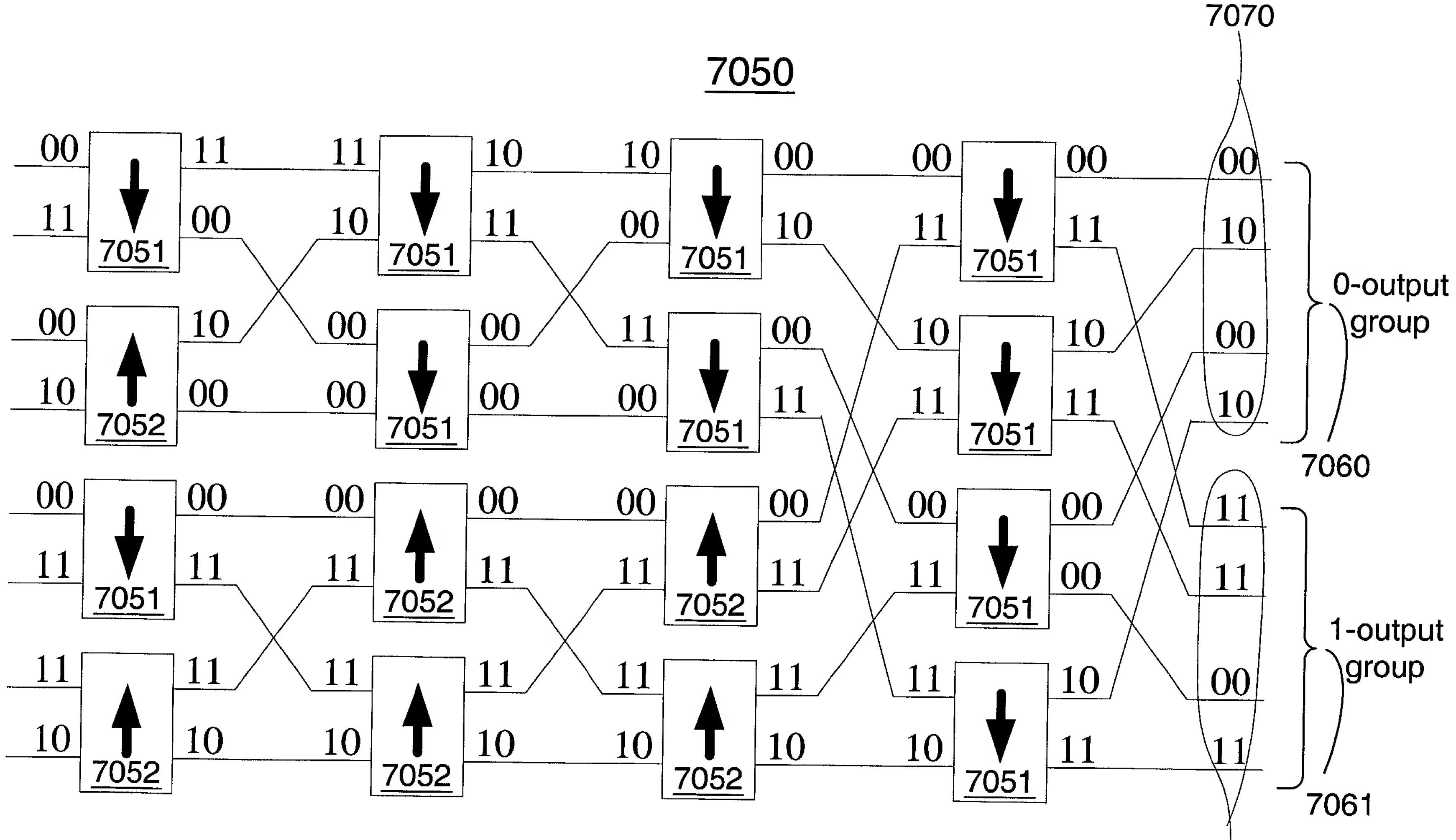

7050
7051
7052
00
11
10
0-output group
1-output group
7060
7061
7070
7071

FIG. 70B

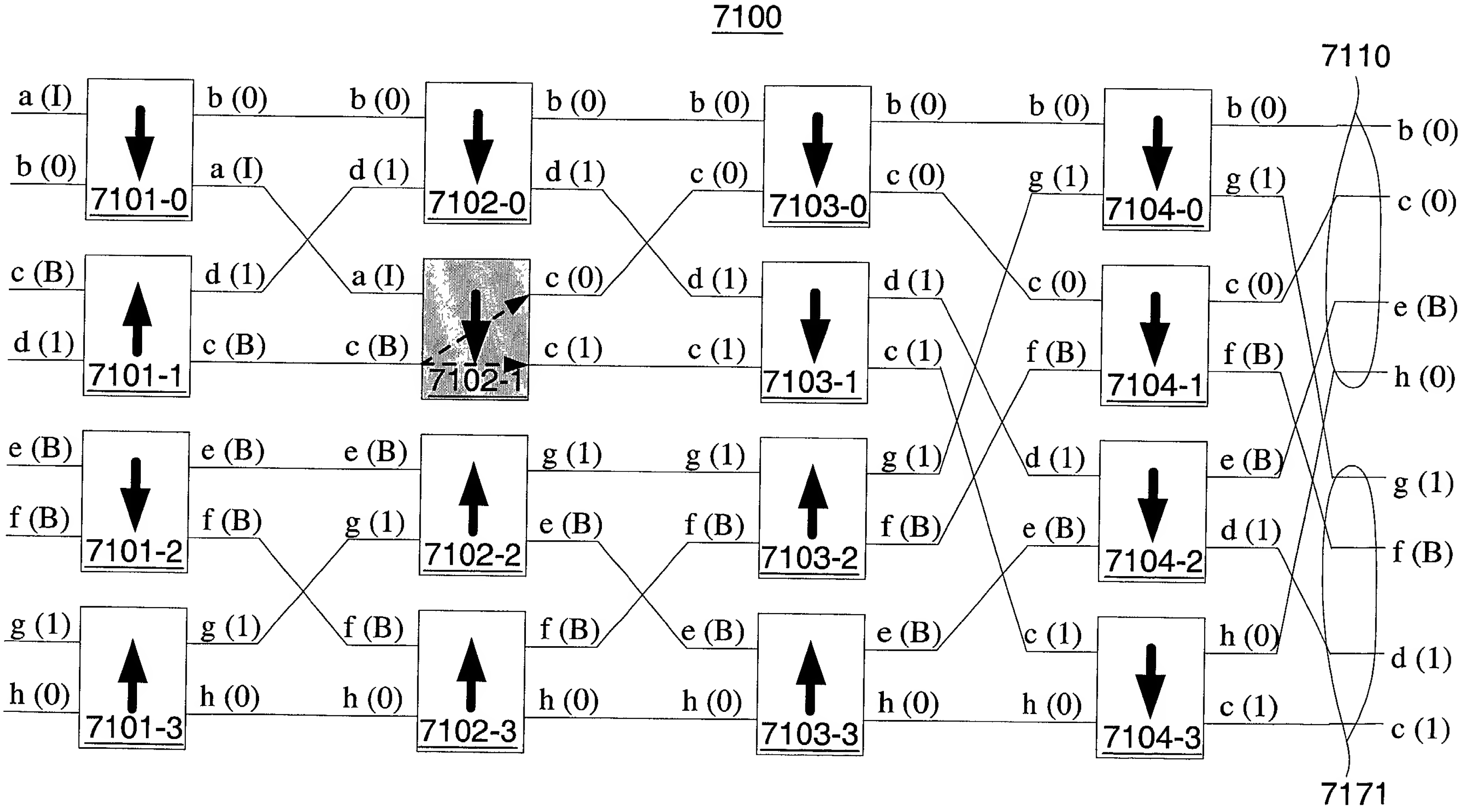

7100
7110
7171
7101-0
7101-1
7101-2
7101-3
7102-0
7102-1
7102-2
7102-3
7103-0
7103-1
7103-2
7103-3
7104-0
7104-1
7104-2
7104-3
a (I)
b (0)
c (B)
d (1)
e (B)
f (B)
g (1)
h (0)
b (0)
a (I)
d (1)
c (B)
e (B)
f (B)
g (1)
h (0)
b (0)
d (1)
a (I)
c (B)
e (B)
g (1)
f (B)
h (0)
b (0)
d (1)
c (0)
c (1)
g (1)
e (B)
f (B)
h (0)
b (0)
c (0)
d (1)
c (1)
g (1)
f (B)
e (B)
h (0)
b (0)
c (0)
d (1)
c (1)
g (1)
f (B)
e (B)
h (0)
b (0)
g (1)
c (0)
f (B)
d (1)
e (B)
c (1)
h (0)
b (0)
g (1)
c (0)
f (B)
e (B)
d (1)
h (0)
c (1)
b (0)
c (0)
e (B)
h (0)
g (1)
f (B)
d (1)
c (1)

FIG. 71A

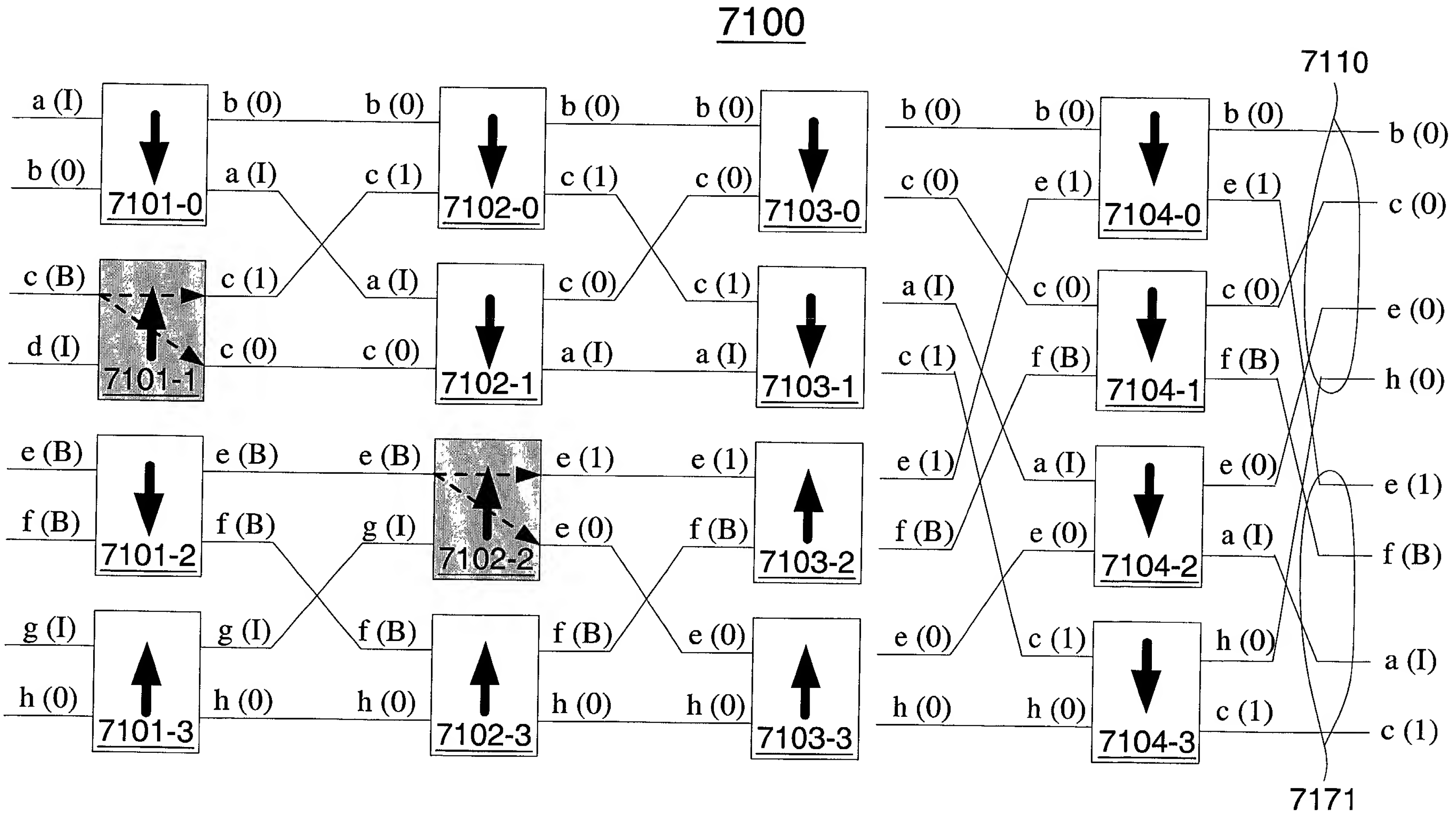

7100
7110
7171
7101-0
7101-1
7101-2
7101-3
7102-0
7102-1
7102-2
7102-3
7103-0
7103-1
7103-2
7103-3
7104-0
7104-1
7104-2
7104-3
a (I)
b (0)
c (B)
d (I)
e (B)
f (B)
g (I)
h (0)
b (0)
a (I)
c (1)
c (0)
e (B)
f (B)
g (I)
h (0)
b (0)
c (1)
a (I)
c (0)
e (B)
g (I)
f (B)
h (0)
b (0)
c (1)
c (0)
a (I)
e (1)
e (0)
f (B)
h (0)
b (0)
c (0)
c (1)
a (I)
e (1)
f (B)
e (0)
h (0)
b (0)
c (0)
a (I)
c (1)
e (1)
f (B)
e (0)
h (0)
b (0)
e (1)
c (0)
f (B)
a (I)
e (0)
c (1)
h (0)
b (0)
e (1)
c (0)
f (B)
e (0)
a (I)
h (0)
c (1)
b (0)
c (0)
e (0)
h (0)
e (1)
f (B)
a (I)
c (1)

FIG. 71B

7200

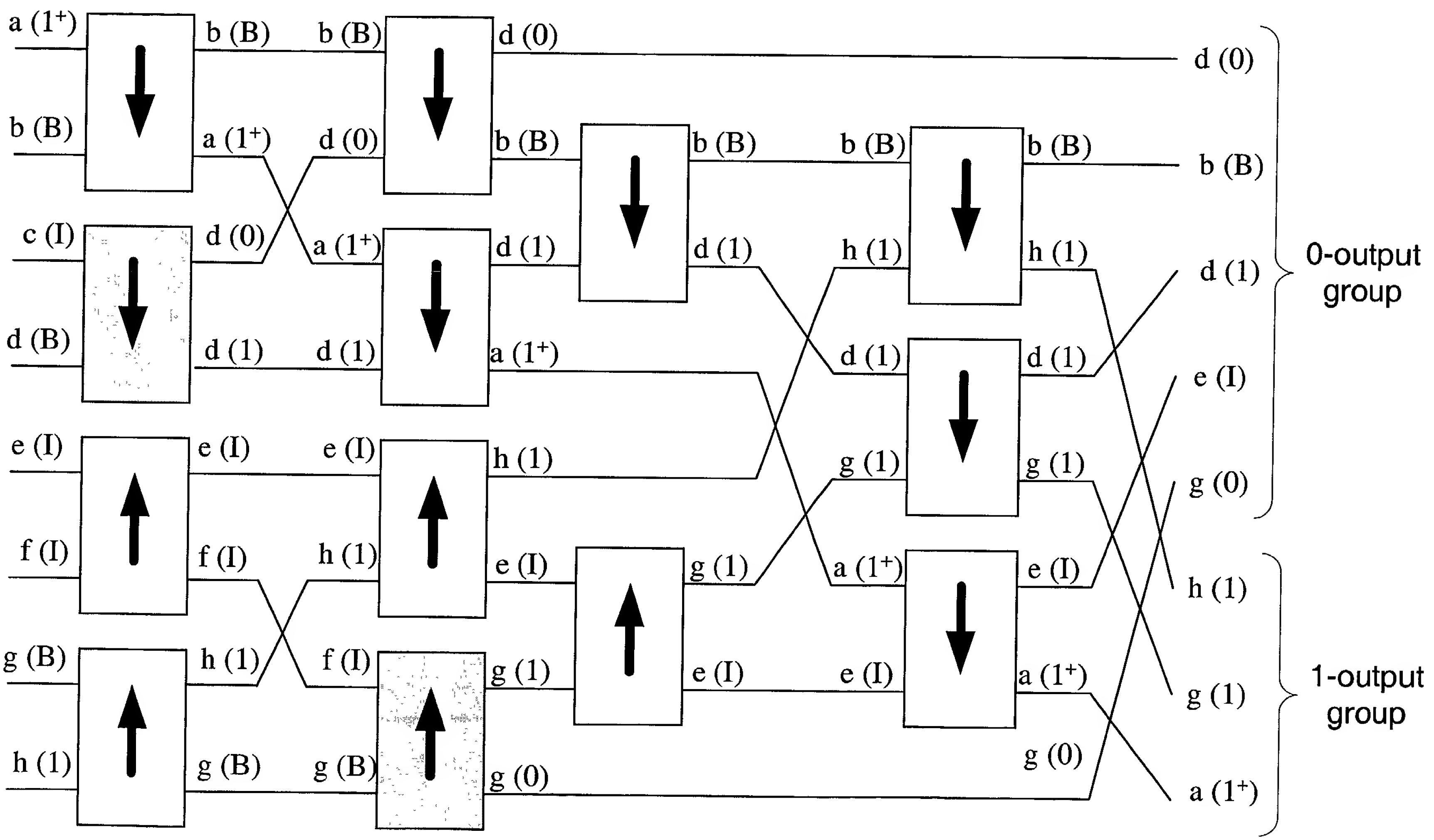

a (1+)
b (B)
c (I)
d (B)
e (I)
f (I)
g (B)
h (1)
b (B)
a (1+)
d (0)
d (1)
e (I)
f (I)
h (1)
g (B)
b (B)
d (0)
a (1+)
d (1)
e (I)
h (1)
f (I)
g (B)
d (0)
b (B)
d (1)
a (1+)
h (1)
e (I)
g (1)
g (0)
b (B)
d (1)
g (1)
e (I)
b (B)
h (1)
d (1)
g (1)
a (1+)
e (I)
b (B)
h (1)
d (1)
g (1)
e (I)
a (1+)
g (0)
d (0)
b (B)
d (1)
e (I)
g (0)
h (1)
g (1)
a (1+)
0-output group
1-output group

FIG. 72A

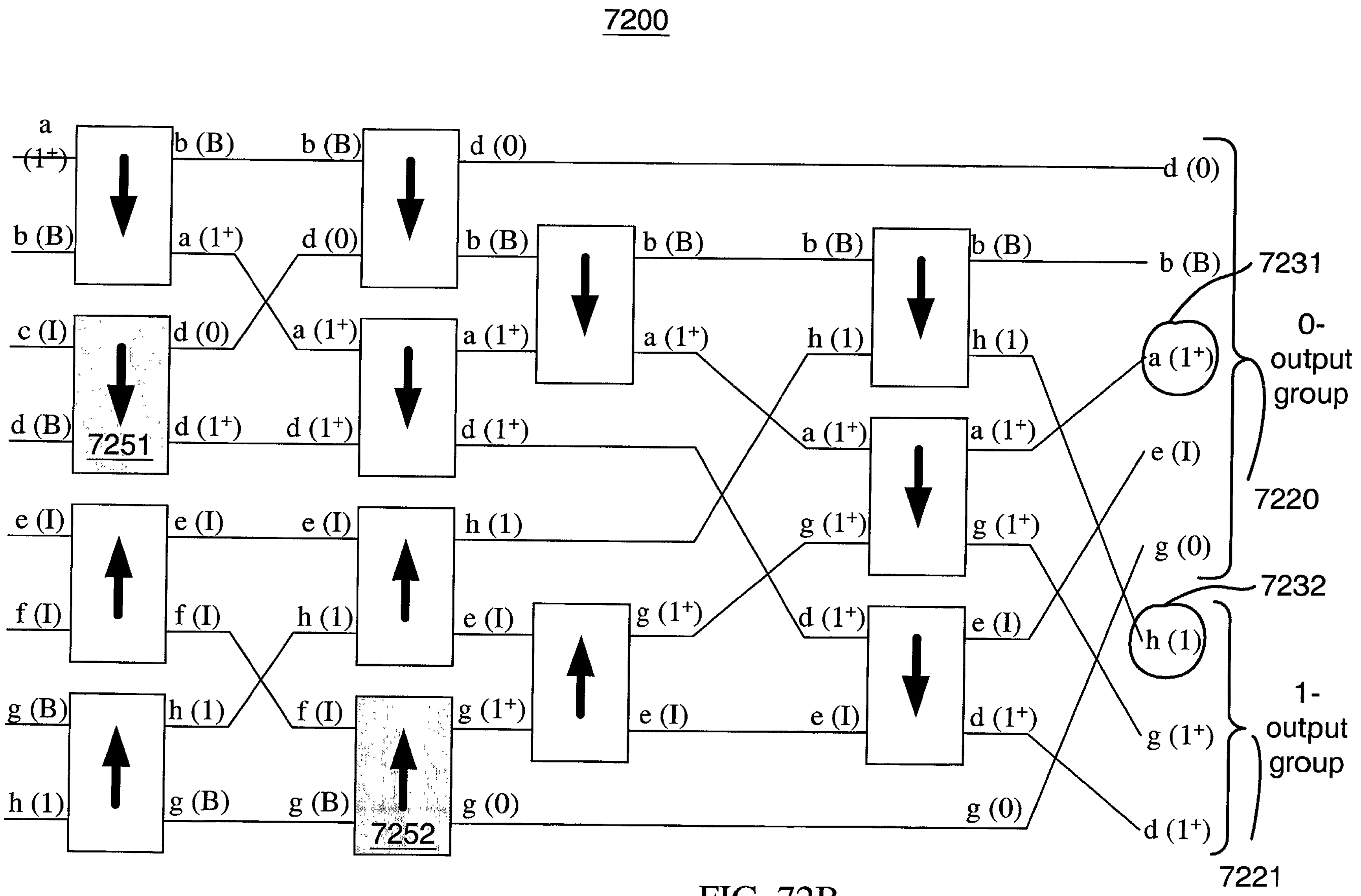

7200
a (1+)
b (B)
c (I)
d (B)
e (I)
f (I)
g (B)
h (1)
7251
7252
b (B)
a (1+)
d (0)
d (1+)
e (I)
f (I)
h (1)
g (B)
d (0)
b (B)
a (1+)
d (1+)
e (I)
h (1)
f (I)
g (B)
d (0)
b (B)
a (1+)
d (1+)
h (1)
e (I)
g (1+)
g (0)
b (B)
a (1+)
g (1+)
e (I)
b (B)
h (1)
a (1+)
g (1+)
d (1+)
e (I)
g (0)
b (B)
h (1)
a (1+)
g (1+)
e (I)
d (1+)
d (0)
b (B)
a (1+)
e (I)
g (0)
h (1)
g (1+)
d (1+)
7231
0-
output
group
7220
7232
1-
output
group
7221

FIG. 72B

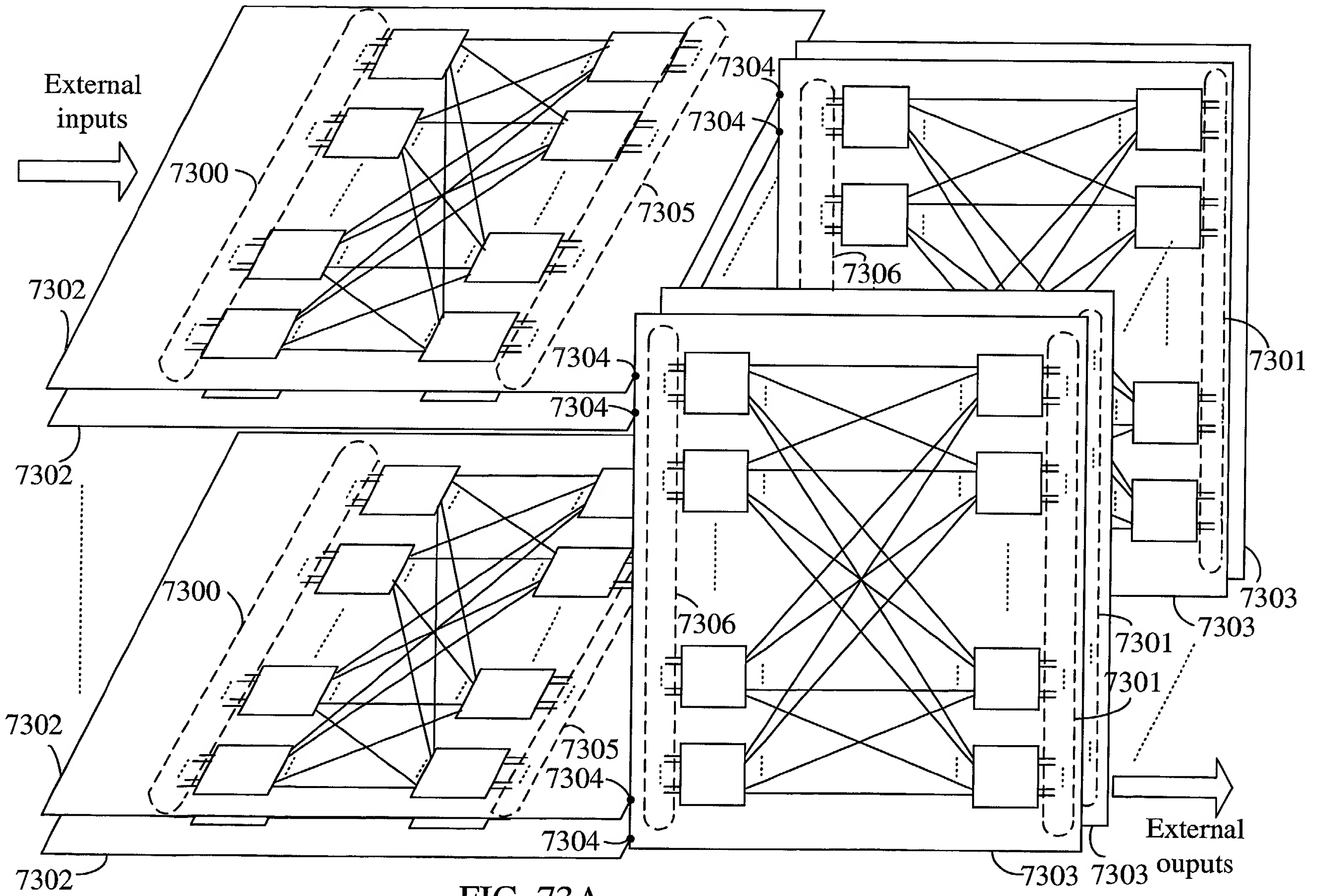
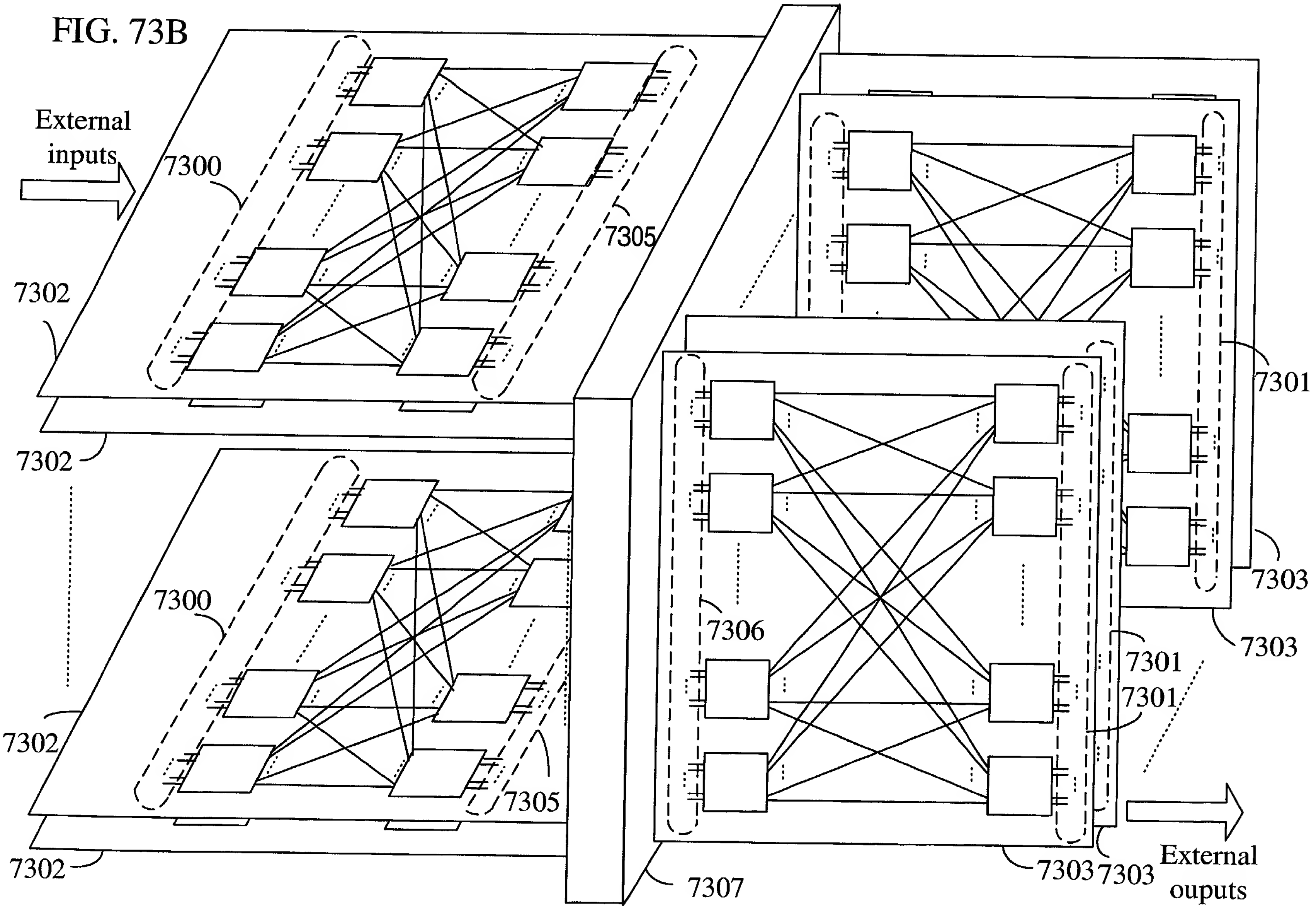

External inputs
7300
7302
7304
7305
7302
7300
7302
7305
7304
7304
7302
7304
7304
7306
7306
7301
7303
7303
7301
7301
7303
7303
External ouputs

FIG. 73A

FIG. 73B


External inputs
7300
7302
7305
7302
7300
7302
7305
7302
7306
7307
7301
7303
7303
7301
7301
7303
7303
External ouputs

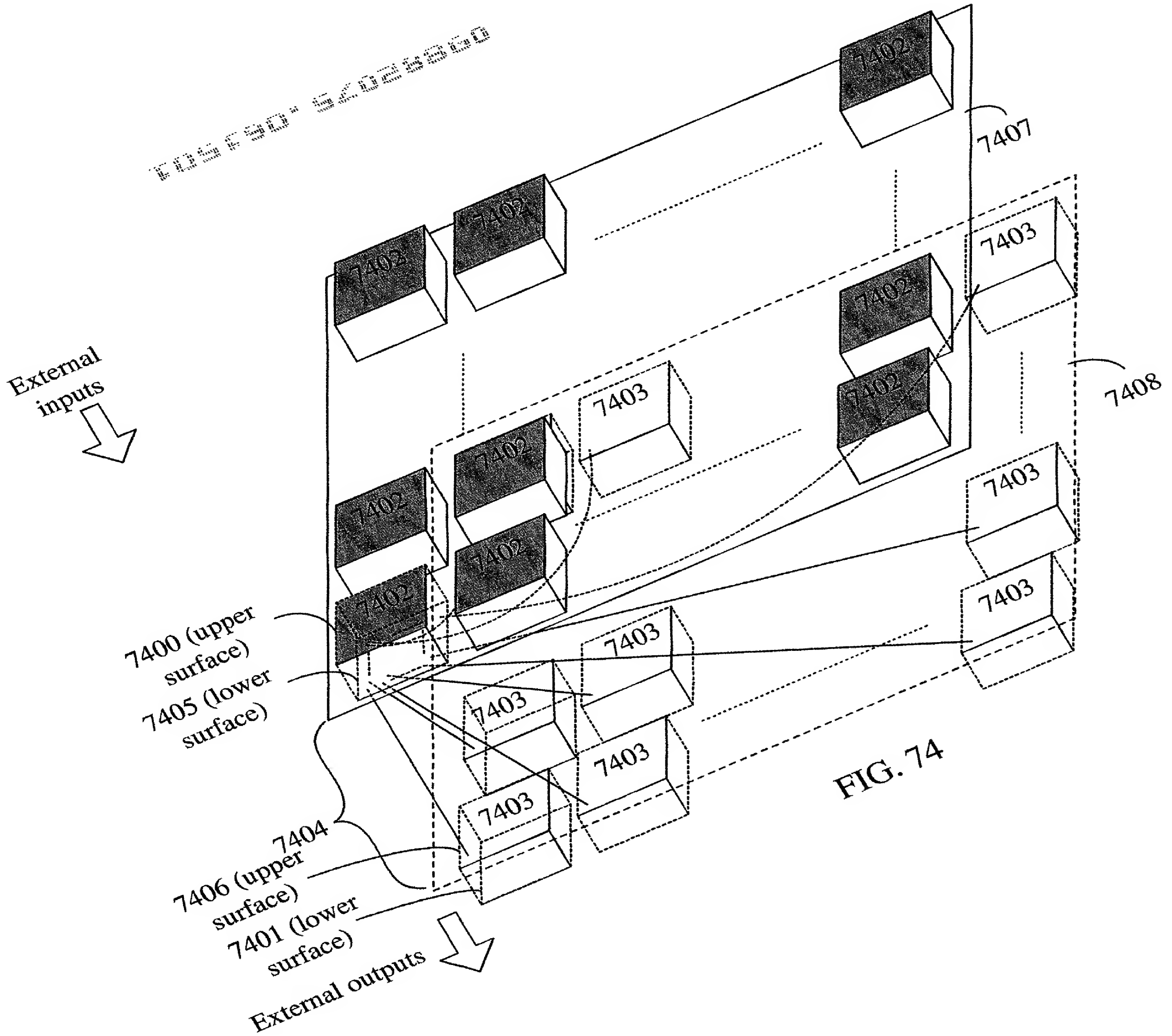

7402
7402
7402
7402
7402
7402
7402
7402
7402
7407
7403
7403
7403
7403
7403
7403
7403
7403
7408
External inputs
7400 (upper surface)
7405 (lower surface)
7404
7406 (upper surface)
7401 (lower surface)
External outputs

FIG. 74

FIG. 75A

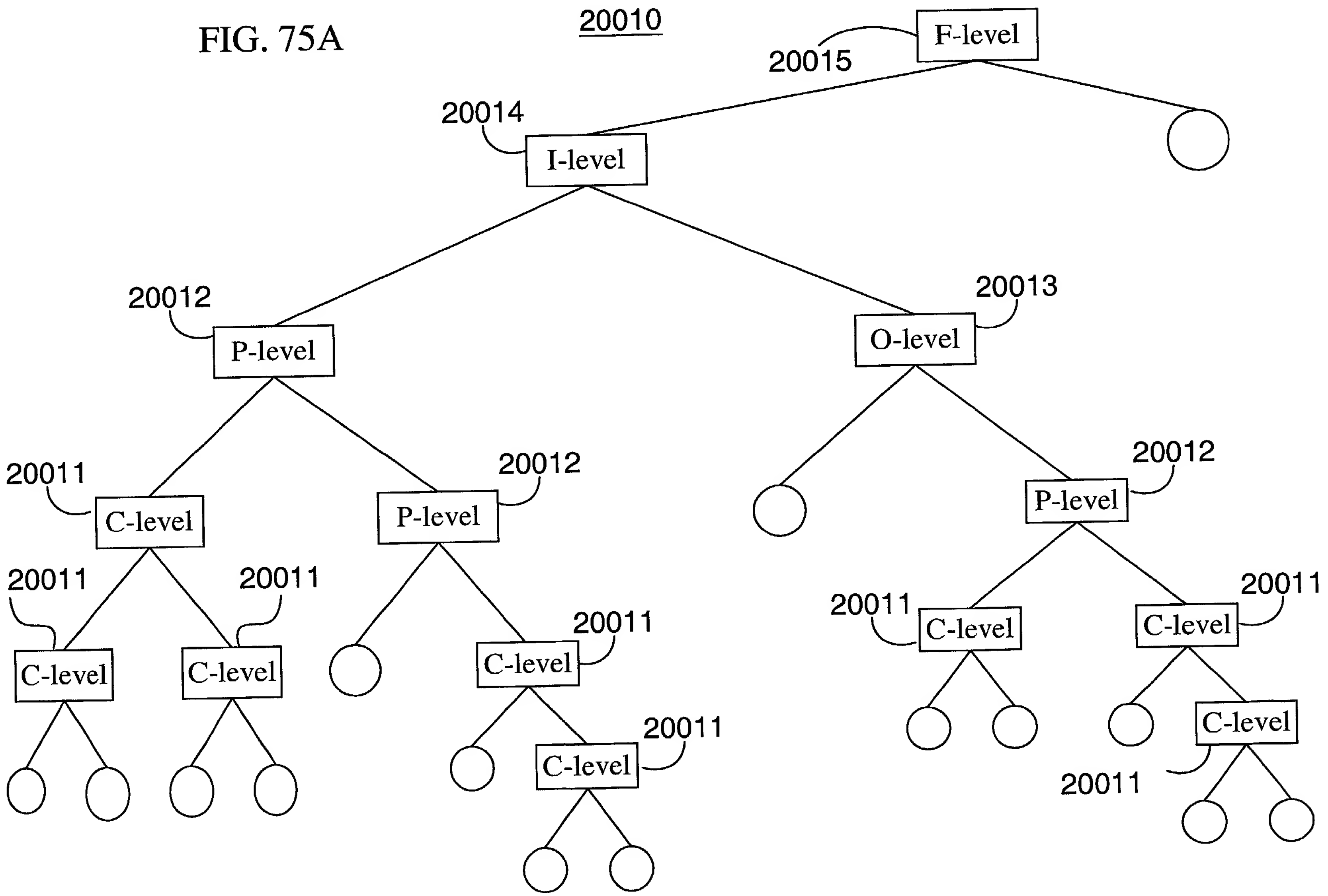

20010
F-level
20015
I-level
20014
P-level
20012
O-level
20013
C-level
20011
P-level
20012
C-level
20011
C-level
20011
C-level
20011
C-level
20011
P-level
20012
C-level
20011
C-level
20011
C-level
20011
C-level
20011

FIG. 75B

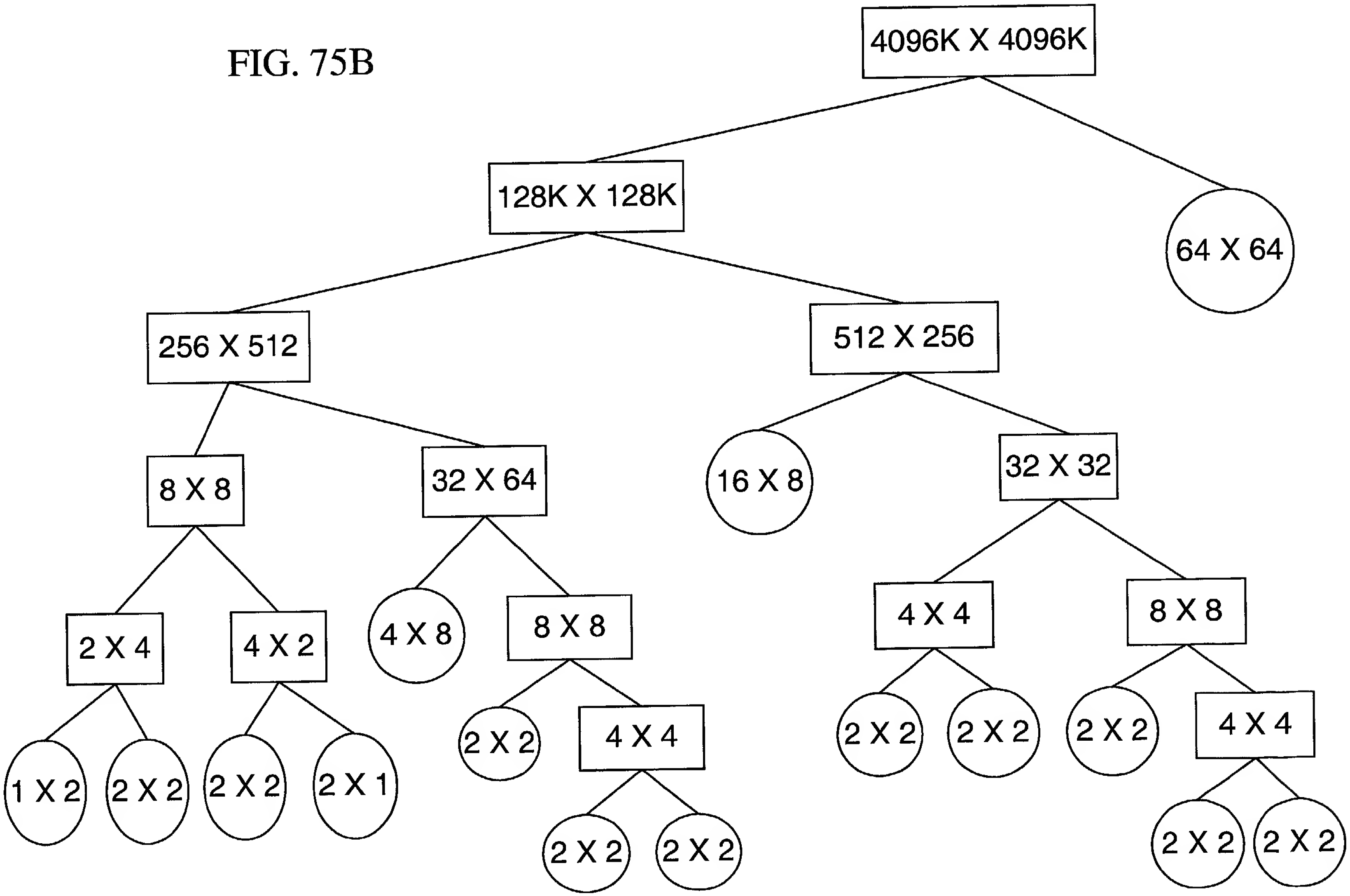
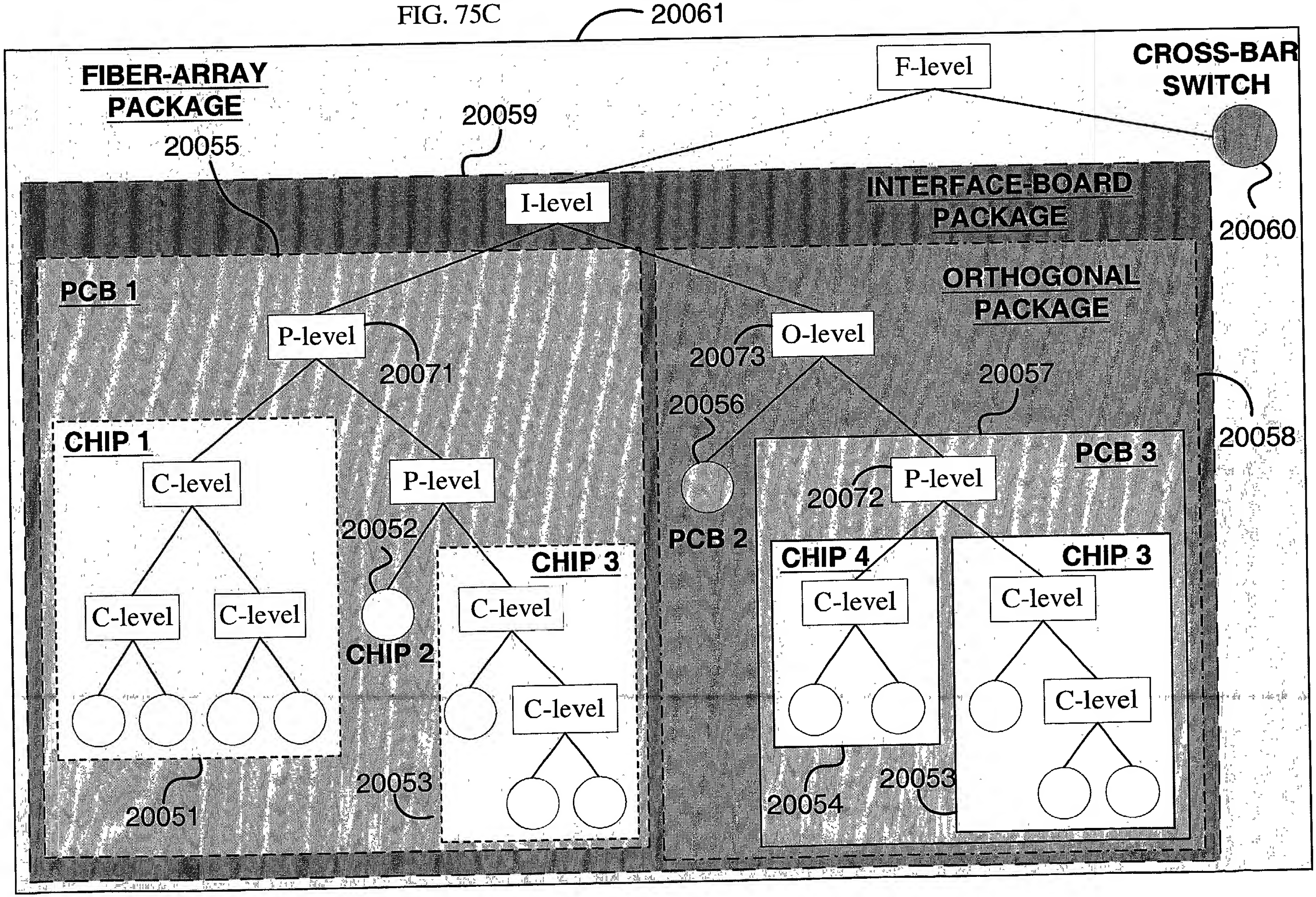

4096K X 4096K
128K X 128K
64 X 64
256 X 512
512 X 256
8 X 8
32 X 64
16 X 8
32 X 32
2 X 4
4 X 2
4 X 8
8 X 8
4 X 4
8 X 8
1 X 2
2 X 2
2 X 2
2 X 1
2 X 2
4 X 4
2 X 2
2 X 2
2 X 2
4 X 4
2 X 2
2 X 2
2 X 2
2 X 2

FIG. 75C


20061
FIBER-ARRAY PACKAGE
20055
20059
F-level
CROSS-BAR SWITCH
20060
I-level
INTERFACE-BOARD PACKAGE
ORTHOGONAL PACKAGE
PCB 1
P-level
20071
O-level
20073
20057
20056
20058
CHIP 1
C-level
P-level
PCB 3
P-level
20072
20052
CHIP 3
PCB 2
CHIP 4
CHIP 3
C-level
C-level
C-level
C-level
C-level
CHIP 2
C-level
C-level
20051
20053
20054
20053